EMFO LIBRARY

TM 11-6625-502-10/3

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

304
EMFO LIBRARY
Changes 1, 2

OPERATOR'S MANUAL

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT

AN/GSM-51, DIGITAL ELEMENT CARD TEST PROCEDURES FOR RADAR PROCESSING CENTER OA-2308/MSQ-28, WEAPONS MONITORING CENTER OA-2309/MSQ-28, AND ELECTRONIC SHOP, SEMITRAILER MOUNTED AN/MSM-34

(Cards numbered 530000 through 548599)

EMFO LIBRARY

HEADQUARTERS, DEPARTMENT OF THE ARMY

JUNE 1963

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on the ac line and dc power connections. Serious injury or death may result from contact with these terminals.

DON'T TAKE CHANCES!

EMFO LIBRARY
18 JAN 19
Changes in force: C 1 and C 2
EMFO LIBRARY

TM 11–6625–502–10/3
C 2

CHANGE
No. 2

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., *2 December 1966*

Operator's Manual

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNITS AN/GSM–51 AND AN/GSM–51A, DIGITAL ELEMENT CARD TEST PROCEDURES FOR RADAR PROCESSING CENTER OA–4333/MSQ–28B, WEAPONS MONITORING CENTER OA–4342/MSQ–28B, AND ELECTRONIC SHOP, SEMITRAILER MOUNTED AN/MSM–34 (CARDS NUMBERED 530000 THROUGH 548599)

TM 11–6625–502–10/3, 15 June 1963, is changed as follows:

Page 17, paragraph 16, below heading. Change "(fig. 4)" to: (fig. 8).

Figure 4, caption. Change "540551" to: 540848.

Page 25, paragraph 20, below heading. Change "(fig. 8)" to: (fig. 4).

Figure 8, caption. Change "540848" to: 540551.

Page 43, paragraph 39. Make the following changes: Delete subparagraph *c* (page 1 of C 1) and substitute:

c. Connect a load between jacks B and DC VOLTAGES 50 with jumper leads, and set LOAD switch to position 8.

Delete subparagraph *d* and substitute:

d. Connect a jumper lead from jack $\overline{Y}$ to DC VOLTAGES 50.

Page 52, paragraph 47 (page 1 of C 1). Delete subparagraphs *b* and *c* and substitute:

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switch M to TRUE.

Page 220, paragraph 201. Make the following changes:

Delete subparagraph (page 1 of C 1) *c* and substitute:

c. Connect LOAD 1 in series between jacks W and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 switch to position 8.

Delete subparagraph *d* and substitute:

d. Connect a jumper lead from jack $\overline{Y}$ to DC VOLTAGES 50.

Page 336, paragraph 302 (page 1 of C 1). Delete subparagraph *b* and *c* and substitute:

b. Press SELECT switch 1 on.

c. Insert matrix assembly 548569 into test jack J1.

By Order of the Secretary of the Army:

HAROLD K. JOHNSON,
General, United States Army,
Chief of Staff.

Official:
KENNETH G. WICKHAM,
Major General, United States Army,
The Adjutant General.

EMFO LIBRARY

Distribution:
To be distributed in accordance with DA Form 12–32, Sec III (Unclas) requirements for Organizational maintenance, AN/FSQ–34, AN/MSG–4, AN/MSQ–18, AN/MSQ–40, AN/TSQ–38, AN/MSQ–38 and AN/MSQ–56 systems.

TAGO 906A—Dec. 250–470°—66

EMFO LIBRARY

U.S. GOVERNMENT PRINTING OFFICE: 1966

EMFO LIBRARY

Changes in force: C 1 and C 2

TM 11-6625-502-10/3
C 2

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., 3 December 1966

Operator's Manual

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNITS AN/GSM-51 AND AN/GSM-51A, DIGITAL ELEMENT CARD TEST PROCEDURES FOR RADAR PROCESSING CENTER OA-4333/MSQ-28B, WEAPONS MONITORING CENTER OA-4342/MSQ-28B, AND ELECTRONIC SHOP, SEMITRAILER MOUNTED AN/MSM-34 (CARDS NUMBERED 530000 THROUGH 548599)

TM 11-6625-502-10/3, 15 June 1963, is changed as follows:

Page 17, paragraph 16, below heading. Change "(fig. 1)" to: (fig. 8).

Figure 4, caption. Change "540551" to: 540848.

Page 25, paragraph 20, below heading. Change "(fig. 3)" to: (fig. 4).

Figure 8, caption. Change "540848" to: 540551.

Page 28, paragraph 39. Make the following changes: Delete subparagraph *a* (page 1 of C 1) and substitute:

a. Connect a load between jacks B and DC VOLTAGES 50 with jumper leads, and set LOAD switch to position 8.

Delete subparagraph *d* and substitute:

d. Connect a jumper lead from jack $\overline{Y}$ to DC VOLTAGES 50.

By Order of the Secretary of the Army:

Page 53, paragraph 47 (page 1 of C 1). Delete subparagraphs *b* and *c* and substitute:

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switch M to TRUE.

Page 220, paragraph 201. Make the following changes:

Delete subparagraph (page 1 of C 1) *c* and substitute:

c. Connect LOAD 1 in series between jacks W and DC VOLTAGES – 50 with jumper leads, and set the LOAD 1 switch to position 8.

Delete subparagraph *d* and substitute:

d. Connect a jumper lead from jack $\overline{Y}$ to DC VOLTAGES 50.

Page 396, paragraph 302 (page 1 of C 1). Delete subparagraph *b* and *c* and substitute:

b. Press SELECT switch 1 on.

c. Insert matrix assembly 548569 into test jack J1.

HAROLD K. JOHNSON,
General, United States Army,
Chief of Staff.

Official:
KENNETH G. WICKHAM,
Major General, United States Army,
The Adjutant General.

Distribution:
To be distributed in accordance with DA Form 12-32, Sec III (Unclas) requirements for Organizational maintenance, AN/FSQ-34, AN/MSG-4, AN/MSQ-18, AN/MSQ-40, AN/TSQ-38, AN/MSQ-38 and AN/MSQ-56 systems.

TAGO 9064 - Dec 280 470 - 66

30 SEP 65
EMFO LIBRARY

TM 11-6625-502-10/3
C 1
1966

CHANGE
No. 1

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., *29 July 1965*

Operator's Manual

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNITS AN/GSM-51 AND AN/GSM-51A, DIGITAL ELEMENT CARD TEST PROCEDURES FOR RADAR PROCESSING CENTER OA-4333/MSQ-28B, WEAPONS MONITORING CENTER OA-4342/MSQ-28B, AND ELECTRONIC SHOP, SEMITRAILER MOUNTED AN/MSM-34 (CARDS NUMBERED 530000 THROUGH 548599)

TM 11-6625-502-10/3, 17 June 1963, is changed as follows:

Title is changed as shown above.

Change paragraphs covering the testing of Matrix Card Assemblies as identified in the table of contents as follows: Delete subparagraphs *b* and *c* and substitute.

b. Connect a jumper lead from jack A to DC VOLTAGES −50.

c. Connect a jumper lead from jack $\overline{Y}$ to DC VOLTAGES 50.

In paragraphs 7 through 27, pages 7 through 31, and paragraphs 29 through 317, pages 35 through 353, add subparagraph *a.1* after subparagraph *a*, as follows:

a.1. Press SPECIAL RELAY/JK/K$\overline{K}$ F/F TEST indicator switch so the JK/K$\overline{K}$ F/F TEST section is not lighted.

Page 5, paragraph 1. Make the following changes:

Subparagraph *a*, line 4. After "AN/GSM-51" add: or AN/GSM-51A.

Subparagraph *b*(3), line 3. Change "593600" to: 599358.

Subparagraph *c*. Delete and substitute.

c. Reporting Equipment Manual Improvements. The direct reporting by the individual user of errors, omissions, and recommendations for improving this manual is authorized and encouraged. DA Form 2028 (Recommended Changes to DA Publications) will be used for reporting these improvements. This form will be completed using pencil, pen, or typewriter and forwarded direct to Commanding General, U.S. Army Electronics Command, ATTN: AMSEL-MR-(NMP)-MA, Fort Monmouth, N.J., 07703.

Page 6, paragraph 5. After subparagraph *e*, add:

e.1. SPECIAL RELAY/JK/K$\overline{K}$ F/F TEST Indicator Switch and Jack J1. In certain test procedures (nonflip-flop cards only), jumper connections are made from the output of the card under test to jack J1 in the tester control panel. Operation of relay K1 is indicated by the lighting of the RELAY indicator of the SPECIAL RELAY/JK/K$\overline{K}$ F/F TEST indicator switch, which is set with the JK/K$\overline{K}$ F/F TEST section not lighted. When testing flip-flop cards, the SPECIAL RELAY/JK/K $\overline{K}$ F/F TEST indicator switch is set so the JK/$\overline{K}$K F/F TEST section is lighted.

Page 33, paragraph 28*b*. After "on," add: and press SPECIAL RELAY/JK/K$\overline{K}$ F/F TEST indicator switch to light the JK/K$\overline{K}$ F/F TEST section.

Page 60, paragraph 52. Make the following changes:

Delete the last sentence in subparagraph *m*.

Redesignate subparagraphs *n* through *y* as subparagraphs *ad* through *ao*.

Redesignate subparagraph *z* as subparagraph *aw*.

Redesignate subparagraph *aa* as subparagraph *ap*.

After subparagraph *m*, add the following:

n. On card assembly, observe that waveform at TPB1-3 corresponds to Waveform Ⓐ, figure 13.1.

o. Set HARMONIZATION S2, on card assembly, to TEST.

p. On card assembly, observe that waveform at TPB1-3 corresponds to waveform Ⓑ, figure 13.1.

q. Return S2, on card assembly, to NORMAL.

r. On card assembly, observe that waveform at TPB1-1 corresponds to waveforms Ⓒ, Ⓓ, and Ⓔ,

figure 13.1, with S1 EQUALIZATION set as shown in the following chart:

Switch	Position	Waveform
S1	0—.5K	Ⓒ
S1	.5—2K	Ⓓ
S1	2—3K	Ⓔ

s. Return switch S1, on card assembly, to 0—.5K.

t. Set S3 DELAY ADJUST, on card assembly, to .4.

u. On card assembly, observe that waveform at TPB1–3 corresponds to waveform Ⓕ, figure 13.1.

v. Set S3, on card assembly, to .6.

w. Observe that the waveform at TPB1–3 is delayed 0.6 microsecond with respect to reference pulse.

x. Set S3, on card assembly, to .8.

y. Observe that the waveform at TPB1–3 is delayed 0.8 microsecond with respect to reference pulse.

z. Set S3, on card assembly, to 1.0.

aa. Observe that the waveform at TPB1–3 is delayed 1.0 microsecond with respect to reference pulse.

ab. Set S3, on card assembly, to 1.2.

ac. Observe that waveform at TPB1–3 is delayed 1.2 microseconds with respect to reference pulse, corresponding to waveform Ⓐ, figure 13.1.

After subparagraph *ap*, add the following:

aq. Measure 97 ohms between jacks *c* and *m*.

ar. Turn R1, on card assembly, fully clockwise.

as. Measure 47 ohms between jacks *c* and *m*.

at. Measure 0 ohm between TPB1–2 on card assembly and jack $\overline{K}$.

au. Set S2, on card assembly, to TEST.

av. Measure 0 ohm between TPB1–2 on card assembly and jack $\overline{N}$.

Add figure 13.1 after subparagraph *aw*.

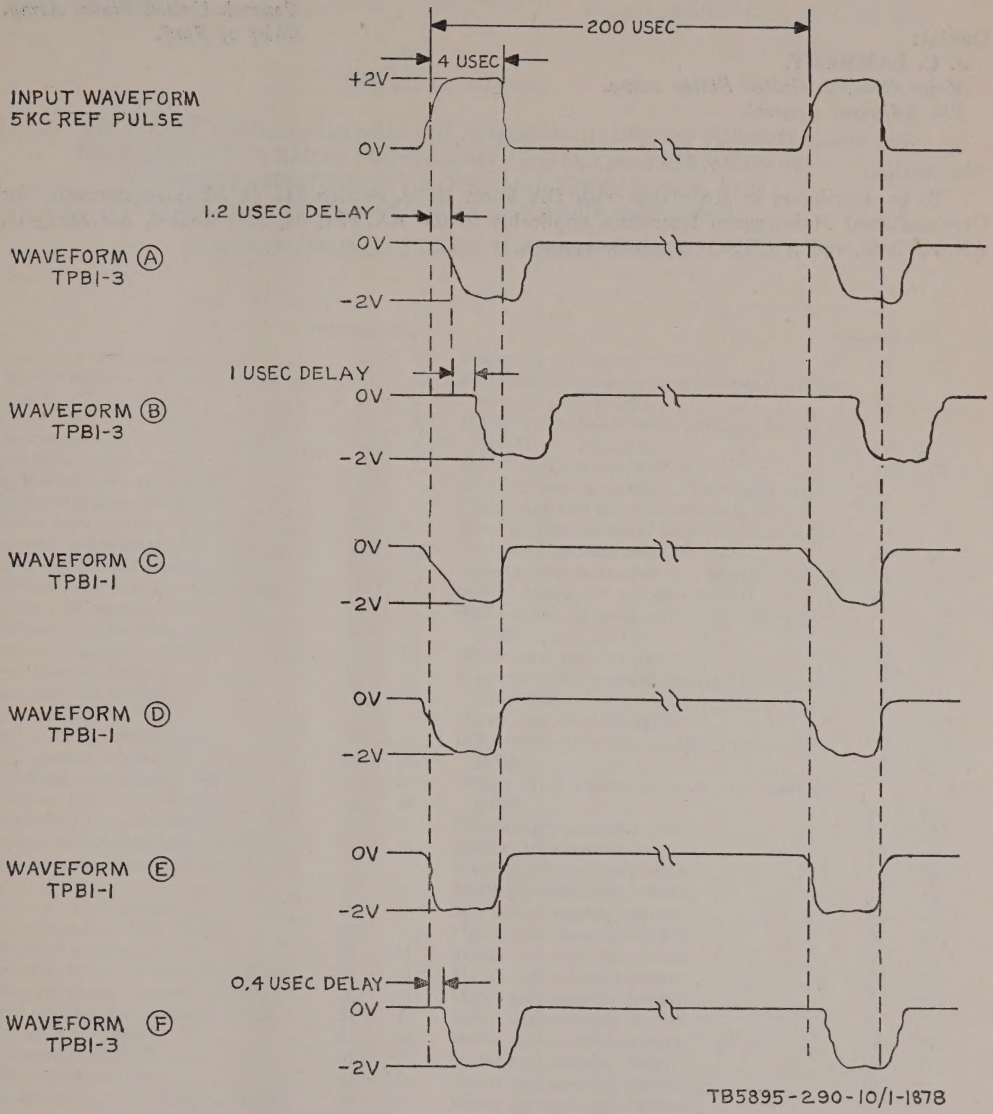


Figure 13.1. IFF/surveillance video amplifier card assem bly 547955, waveform diagram.

By Order of the Secretary of the Army:

HAROLD K. JOHNSON,
General, United States Army,
Chief of Staff.

Official:
J. C. LAMBERT,
Major General, United States Army,
The Adjutant General.

Distribution:
To be distributed in accordance with DA Form 12–32, Section III (Unclas) requirements for Organizational Maintenance Literature applicable to the AN/FSQ–34, AN/MSG–4, AN/MSQ–18, AN/MSQ–40, and AN/TSQ–38 missile systems.

U.S. GOVERNMENT PRINTING OFFICE: 1965

TECHNICAL MANUAL
No. 11-6625-502-10/3

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D.C., *17 June, 1963*

LMFO LIBRARY

OPERATOR'S MANUAL

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT AN/GSM-51, DIGITAL ELEMENT CARD TEST PROCEDURES FOR RADAR PROCESSING CENTER OA-2308/MSQ-28, WEAPONS MONITORING CENTER OA-2309/MSQ-28, AND ELECTRONIC SHOP, SEMITRAILER MOUNTED AN/MSM-34

(CARDS NUMBERED 530000 THROUGH 548599)

	Paragraph	Page
Scope	1	5
Index of publications	2	5
Use of manual	3	5
Test equipment	4	5
General instructions	5	5
Test procedures	6	6
Write amplifier card assembly 530231	7	7
Read amplifier card assembly 533094	8	9
Gate amplifier card assembly 534001	9	11
Logic converter card assembly 534393	10	11
14-Core shift register card assembly 534770	11	12
6.8K Emitter follower card assembly 534930	12	12
Servoamplifier card assembly 539657	13	13
Emitter follower card assembly 539818	14	15
Trigger gate card assembly 539857	15	15
Matrix card assembly 540551	16	17
Matrix card assembly 540553	17	19
Matrix card assembly 540555	18	21
Matrix card assembly 540557	19	23
Matrix card assembly 540848	20	25
Blocking oscillator card assembly 542303	21	27
Sweep switch card assembly 543928	22	29
Digilog switch card assembly 543929	23	29
Digilog resistor network card assembly 544592	24	30
Digit square wave generator card assembly 546643	25	30
Amplifier card assembly 546804	26	30
Hybrid network card assembly 546806	27	31
Fast flip-flop card assembly 547514	28	33
Video coaxial line driver card assembly 547536	29	35
Analog sweep switch card assembly 547716	30	35
Light control amplifier card assembly 547724	31	35
Matrix card assembly 547864	32	36
Matrix card assembly 547865	33	37
Switch card assembly 547866	34	38
Skimmer matrix and test card assembly 547867	35	40
Up-down counter stop and test card assembly 547869	36	41
Range gate and video skimmer card assembly 547870	37	42
Digilog and blocking oscillator card assembly 547872	38	43
Matrix card assembly 547874	39	43
RHI video intensity blanking pedestal generator card assembly 547875	40	45
Marker and azimuth cursor gate card assembly 547876	41	47
Matrix card assembly 547878	42	47
Azimuth cursor generator card assembly 547879	43	49
Composite video gate card assembly 547880	44	51
Process ATWS video and height blanking pedestal generator card assembly 547882	45	51
Direct current power filter card assembly 547885	46	52
Special matrix card assembly 547901	47	52
RHI intensity pedestal switch card assembly 547947	48	54
Matrix card assembly 547948	49	54
Marker intensity pedestal generator card assembly 547949	50	57
Matrix card assembly 547950	51	59
IFF/surveillance video amplifier card assembly 547955	52	60
HFR 1/HFR 2 video amplifier card assembly 547957	53	60
Matrix card assembly 548000	54	61
Matrix card assembly 548001	55	62
Matrix card assembly 548002	56	63
Matrix card assembly 548003	57	64
Matrix card assembly 548004	58	66
Matrix card assembly 548005	59	67
Matrix card assembly 548006	60	68
Matrix card assembly 548007	61	70
Matrix card assembly 548008	62	70
Matrix card assembly 548009	63	72
Matrix card assembly 548010	64	73
Matrix card assembly 548011	65	74
Matrix card assembly 548012	66	74
Matrix card assembly 548014	67	75
Matrix card assembly 548016	68	77
Matrix card assembly 548018	69	78
Matrix card assembly 548020	70	78
Matrix card assembly 548022	71	79
Matrix card assembly 548024	72	80
Matrix card assembly 548027	73	82

	Paragraph	Page
Matrix card assembly 548039	74	83
Matrix card assembly 548041	75	84
Matrix card assembly 548042	76	85
Matrix card assembly 548043	77	86
Matrix card assembly 548069	78	87
Matrix card assembly 548071	79	88
Matrix card assembly 548072	80	89
Matrix card assembly 548073	81	90
Matrix card assembly 548074	82	91
Matrix card assembly 548076	83	92
Matrix card assembly 548078	84	93
Matrix card assembly 548082	85	95
Matrix card assembly 548085	86	96
Matrix card assembly 548087	87	97
Matrix card assembly 548089	88	98
Matrix card assembly 548091	89	99
Matrix card assembly 548093	90	100
Matrix card assembly 548095	91	101
Matrix card assembly 548117	92	102
Matrix card assembly 548119	93	104
Matrix card assembly 548121	94	105
Matrix card assembly 548122	95	106
Matrix card assembly 548123	96	107
Matrix card assembly 548124	97	108
Matrix card assembly 548126	98	109
Matrix card assembly 548128	99	110
Matrix card assembly 548130	100	112
Matrix card assembly 548132	101	113
Matrix card assembly 548134	102	114
Matrix card assembly 548136	103	116
Matrix card assembly 548138	104	117
Matrix card assembly 548140	105	118
Matrix card assembly 548142	106	119
Matrix card assembly 548144	107	120
Matrix card assembly 548146	108	121
Matrix card assembly 548148	109	122
Matrix card assembly 548151	110	123
Matrix card assembly 548153	111	124
Matrix card assembly 548155	112	125
Matrix card assembly 548157	113	126
Matrix card assembly 548159	114	127
Matrix card assembly 548161	115	128
Matrix card assembly 548163	116	129
Matrix card assembly 548165	117	130
Matrix card assembly 548167	118	131
Matrix card assembly 548169	119	132
Matrix card assembly 548171	120	134
Matrix card assembly 548173	121	134
Matrix card assembly 548175	122	136
Matrix card assembly 548177	123	136
Matrix card assembly 548179	124	137
Matrix card assembly 548183	125	138
Matrix card assembly 548185	126	140
Matrix card assembly 548187	127	141
Matrix card assembly 548189	128	142
Matrix card assembly 548191	129	143
Matrix card assembly 548192	130	144
Matrix card assembly 548197	131	145
Matrix card assembly 548199	132	146
Matrix card assembly 548201	133	147
Matrix card assembly 548205	134	149
Matrix card assembly 548207	135	150
Matrix card assembly 548208	136	151
Matrix card assembly 548209	137	152
Matrix card assembly 548210	138	153
Matrix card assembly 548211	139	154
Matrix card assembly 548212	140	156
Matrix card assembly 548214	141	157
Matrix card assembly 548215	142	158
Matrix card assembly 548217	143	159
Matrix card assembly 548219	144	160
Matrix card assembly 548222	145	161
Matrix card assembly 548224	146	162
Matrix card assembly 548226	147	163
Matrix card assembly 548228	148	164
Matrix card assembly 548229	149	165
Matrix card assembly 548231	150	166
Matrix card assembly 548233	151	167
Matrix card assembly 548235	152	168
Matrix card assembly 548237	153	169
Matrix card assembly 548239	154	170
Matrix card assembly 548241	155	172
Matrix card assembly 548243	156	172
Matrix card assembly 548245	157	173
Matrix card assembly 548247	158	174
Matrix card assembly 548250	159	175
Matrix card assembly 548251	160	176
Matrix card assembly 548253	161	177
Matrix card assembly 548256	162	179
Matrix card assembly 548258	163	180
Matrix card assembly 548260	164	181
Matrix card assembly 548262	165	182
Matrix card assembly 548264	166	183
Matrix card assembly 548266	167	184
Matrix card assembly 548268	168	185
Matrix card assembly 548274	169	186
Matrix card assembly 548276	170	187
Matrix card assembly 548278	171	188
Matrix card assembly 548280	172	189
Matrix card assembly 548282	173	191
Matrix card assembly 548284	174	192
Matrix card assembly 548287	175	193
Matrix card assembly 548289	176	195
Matrix card assembly 548291	177	196
Matrix card assembly 548292	178	197
Matrix card assembly 548294	179	198
Matrix card assembly 548296	180	199
Matrix card assembly 548298	181	200
Matrix card assembly 548300	182	201
Matrix card assembly 548302	183	202
Matrix card assembly 548304	184	202
Matrix card assembly 548306	185	204
Matrix card assembly 548308	186	205
Matrix card assembly 548310	187	206
Matrix card assembly 548312	188	207
Matrix card assembly 548314	189	208
Matrix card assembly 548316	190	209
Matrix card assembly 548318	191	210
Matrix card assembly 548320	192	211
Matrix card assembly 548322	193	212
Matrix card assembly 548324	194	213
Matrix card assembly 548326	195	214
Matrix card assembly 548328	196	215
Matrix card assembly 548330	197	216

	Paragraph	Page
Matrix card assembly 548332	198	217
Matrix card assembly 548334	199	218
Matrix card assembly 548336	200	219
Matrix card assembly 548338	201	220
Matrix card assembly 548340	202	222
Matrix card assembly 548343	203	223
Matrix card assembly 548344	204	224
Matrix card assembly 548347	205	225
Matrix card assembly 548348	206	227
Matrix card assembly 548350	207	228
Matrix card assembly 548352	208	229
Matrix card assembly 548354	209	230
Matrix card assembly 548356	210	232
Matrix card assembly 548358	211	233
Matrix card assembly 548360	212	234
Matrix card assembly 548362	213	235
Matrix card assembly 548364	214	236
Matrix card assembly 548366	215	237
Matrix card assembly 548368	216	238
Matrix card assembly 548370	217	239
Matrix card assembly 548372	218	240
Matrix card assembly 548392	219	241
Matrix card assembly 548394	220	242
Matrix card assembly 548396	221	244
Matrix card assembly 548398	222	245
Matrix card assembly 548400	223	246
Matrix card assembly 548402	224	247
Matrix card assembly 548404	225	248
Matrix card assembly 548406	226	249
Matrix card assembly 548409	227	250
Matrix card assembly 548411	228	251
Matrix card assembly 548413	229	253
Matrix card assembly 548415	230	253
Matrix card assembly 548417	231	255
Matrix card assembly 548419	232	256
Matrix card assembly 548421	233	257
Matrix card assembly 548423	234	258
Matrix card assembly 548425	235	259
Matrix card assembly 548427	236	260
Matrix card assembly 548429	237	261
Matrix card assembly 548431	238	262
Matrix card assembly 548432	239	263
Matrix card assembly 548438	240	264
Matrix card assembly 548440	241	265
Matrix card assembly 548445	242	266
Matrix card assembly 548447	243	267
Matrix card assembly 548449	244	268
Matrix card assembly 548451	245	269
Matrix card assembly 548453	246	270
Matrix card assembly 548455	247	272
Matrix card assembly 548457	248	273
Matrix card assembly 548459	249	274
Matrix card assembly 548460	250	274
Matrix card assembly 548464	251	276
Matrix card assembly 548466	252	277
Matrix card assembly 548468	253	278
Matrix card assembly 548470	254	279
Matrix card assembly 548472	255	280
Matrix card assembly 548474	256	282
Matrix card assembly 548476	257	283
Matrix card assembly 548478	258	284
Matrix card assembly 548480	259	285
Matrix card assembly 548482	260	287
Matrix card assembly 548484	261	288
Matrix card assembly 548486	262	289
Matrix card assembly 548488	263	291
Matrix card assembly 548490	264	292
Matrix card assembly 548492	265	293
Matrix card assembly 548494	266	294
Matrix card assembly 548496	267	296
Matrix card assembly 548498	268	297
Matrix card assembly 548502	269	298
Matrix card assembly 548504	270	299
Matrix card assembly 548506	271	300
Matrix card assembly 548508	272	301
Matrix card assembly 548510	273	303
Matrix card assembly 548512	274	305
Matrix card assembly 548514	275	306
Matrix card assembly 548516	276	307
Matrix card assembly 548518	277	308
Matrix card assembly 548520	278	309
Matrix card assembly 548522	279	311
Matrix card assembly 548524	280	311
Matrix card assembly 548526	281	313
Matrix card assembly 548528	282	314
Matrix card assembly 548530	283	314
Matrix card assembly 548532	284	316
Matrix card assembly 548534	285	317
Matrix card assembly 548536	286	318
Matrix card assembly 548538	287	319
Matrix card assembly 548540	288	320
Matrix card assembly 548542	289	321
Matrix card assembly 548544	290	322
Matrix card assembly 548546	291	324
Matrix card assembly 548548	292	325
Matrix card assembly 548550	293	326
Matrix card assembly 548552	294	327
Matrix card assembly 548554	295	329
Matrix card assembly 548556	296	330
Matrix card assembly 548558	297	331
Matrix card assembly 548560	298	332
Matrix card assembly 548562	299	333
Matrix card assembly 548564	300	334
Matrix card assembly 548566	301	335
Special matrix card assembly 548569	302	336
Matrix card assembly 548571	303	337
Matrix card assembly 548573	304	338
Matrix card assembly 548575	305	339
Matrix card assembly 548577	306	340
Matrix card assembly 548579	307	341
Matrix card assembly 548581	308	342
Matrix card assembly 548583	309	343
Matrix card assembly 548585	310	344
Matrix card assembly 548587	311	345
Matrix card assembly 548589	312	346
Matrix card assembly 548591	313	347
Matrix card assembly 548592	314	348
Matrix card assembly 548594	315	349
Matrix card assembly 548596	316	350
Matrix card assembly 548598	317	350

1. Scope

a. General. This manual, TM 11–6625–502–10/4, and TM-6625-502-10/5 contain the step-by-step procedures to be followed when using Test Set, Electronic Circuit Plug-in Unit AN/GSM-51 (tester) to test digital element cards in the equipments listed below.

(1) Radar Processing Center OA–2308/MSQ–28.
(2) Weapons Monitoring Center OA–2309/MSQ–28.
(3) Receiver-Transmitter, Digital Data R–1101/MSQ–28.
(4) Electronic Shop, Semitrailer Mounted AN/MSM–34.
(5) Test Set, Circulator Head Setter TS–1687/MSM–34.
(6) Test Set, Electronic Circuit Plug-in Unit TS–1712/MSQ–28.

Note. Description, installation, general operating instructions, operator's preventive maintenance, and the basic issue item list are in TM–11–6625–502–10, Operator's Manual, Test Set, Electronic Circuit Plug-in Unit AN/GSM–51.

b. Manuals. The digital element cards are indexed in these manuals in the order of their six-digit manufacturing identification number:

(1) *TM 11–6625–502–10/3.* This manual contains the procedures for testing the cards numbered from 530000 to 548599.
(2) *TM 11-6625-502-10/4.* This manual contains the procedures for testing the cards numbered from 549600 to 593599.
(3) *TM 11-6625-502-10/5.* This manual contains the procedures for testing the cards numbered 593600 or higher.

c. Comments. Forward all comments on this publication direct to: Commanding Officer, U. S. Army Electronics Materiel Support Agency, ATTN: SELMS-MP, Fort Monmouth, N. J. (DA Form 1598 (Record of Comments on Publications). DA Form 2496 (Disposition Form), or letter may be used.)

d. Forms and Records. For applicable forms and records, see paragraph 2, TM 11–6625–502–10.

2. Index of Publications

Refer to the latest issue of DA Pam 310–4 to determine whether there are new editions, changes, or additional publications pertaining to your equipment. DA Pam 310–4 is a current index of technical manuals, technical bulletins, supply bulletins, lubrication orders, and modification work orders that are available through publications supply channels. The index lists the individual parts (–10, –20, –35P, etc.) and the latest changes to and revisions of each equipment publication.

3. Use of Manual

The cards are identified by six-digit manufacturer's assembly numbers which are stamped on the cards. The card test procedures in this manual are arranged in numerical order. The wave shapes that go with these tests are with the test procedure. If the schematic diagram for a card is not with the card test procedure, it will be found in at least one of two sources, TM 11–5840–271–30/20, Radar Data Processing Center OA-2308/MSQ-28 Card Assembly Schematic Diagrams (U) (RDPC card schematic diagrams) or TM 11 5840-272-30/19, Weapons Monitoring Center OA-2309/MSQ-28 Card Assembly Schematic Diagrams (U) (WMC card schematic diagrams). The referencing to one or the other, or both, of these volumes is indicated after the heading of each test procedure affected.

4. Test Equipment

Use Oscilloscope AN/USM–81 (oscilloscope) or equivalent to observe the waveforms. Refer to TM 11–6625–219–12 for operation of the oscilloscope. Use Electronic Multimeter TS–505B/U (multimeter) to make all voltage and resistance measurements. Refer to TM 11–6625–239–12 for operation of the multimeter.

5. General Instructions

a. Operator's Manual. Refer to TM 11-6625-502-10 for general operating instructions for the tester.

b. Voltage Measurements. Unless otherwise indicated in the test procedure, make all voltage measurements between the indicated jack and GRD jacks.

c. Test Leads. Use the test leads located in the test lead STORAGE compartment in Test Set Sub-Assembly MX–3505/GSM–51 (tester console) for making jumper lead connections.

d. MULTIPLES Jacks. The MULTIPLES jacks on the tester control panel can be used as common connection points to extend jumper leads, or to make jumper connections from a single jack to two or more other jacks.

e. SPECIAL RELAY Indicator and Jack K1. In certain of the test procedures, jumper connections are made from the output of the card under test to jack K1 in the tester control panel. Operation of

relay K1 is indicated by lighting of the SPECIAL RELAY lamp.

f. Synchronizing Signal. The SYNC SIGNAL jack on the tester signal panel provides a connection for synchronizing the oscilloscope with the REF PULSE, DELAY PULSE, or CLOCK PULSE. The synchronizing signal is applied to the SYNC SIGNAL jack when the desired pulse switch is pressed *on*. The WORD SYNC jack provides a signal for synchronizing the oscilloscope with the RANDOM WORD GENERATOR output.

g. Word Selection. Any word combination can be selected by means of the RANDOM WORD GENERATOR bit switches. Not necessarily all 16 digits are used to produce a word.

h. Power Switches. The POWER ON switch turns power to the tester console *on* and *off* and provides potentials for pulse forming without use of the ENERGIZE switch. The ENERGIZE switch turns voltages *on* and *off* to the card under test and the associated test jacks.

i. Load Connections. Two identical sets of 12 resistive loads and a LOAD selector switch for each set are provided. The load can be series- or parallel-connected to obtain other values of resistance. The value of resistance selected is determined by the switch position as follows:

Switch positions	Load resistance
1	150 ohms
2	470 ohms
3	1K
4	4.7K
5	10K
6	22K
7	47K
8	100K
9	220K
10	1 meg
11	51 ohms
12	200 ohms

j. Filament Voltage. When 6.3-volt ac filament voltage is required in the test procedure, a warmup time must be allowed after the ENERGIZE switch is pressed *on*.

***Warning:* To prevent personal injury, or damage to the card under test or to the tester, press the ENERGIZE switch off before making a jumper lead connection or before moving a jumper lead from one jack position to another, unless otherwise instructed.**

6. Test Procedures

Note. The procedures for testing individual digital element cards are given in paragraphs 7 through 317.

a. Perform the preliminary starting procedure given in TM 11–6625–502–10.

b. Insert the card to be tested into the test jack indicated in the test procedure.

***Caution:* Make sure that the pin designations on the card match the designations on the jack when inserting the card.**

7. Write Amplifier Card Assembly 530231

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Press VOLTAGES switches −28, 28, −50, and and 50 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches M and U to TRUE and C and K to FALSE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 170.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

f. Connect a jumper lead from jack to SIGNALS CLOCK PULSE.

g. Insert card assembly 530231 into test jack J1.

h. Press the ENERGIZE switch on.

i. Observe that the waveform at jack B corresponds to the output waveform shown on figure 1.

j. Set TRUE-FALSE switch U to FALSE. Observe that the waveform at jack B disappears.

k. Set TRUE-FALSE switches U, C, and K to TRUE. Observe that waveform at jack B disappears.

l. Set TRUE-FALSE switch K to FALSE. Observe that the waveform at B corresponds to the output waveform shown on figure 1.

m. Set TRUE-FALSE switches K to TRUE, and C to FALSE. Observe that the waveform at B corresponds to the output waveform shown on figure 1.

n. Set TRUE-FALSE switches $\overline{U}$ and $\overline{W}$ to FALSE, and $\overline{K}$ to TRUE.

o. Remove the jumper lead from jack W and connect to jack $\overline{C}$.

p. Observe that the waveform at jack $\overline{X}$ corresponds to the output waveform shown on figure 1.

q. Set TRUE-FALSE switch $\overline{K}$ to FALSE. Observe that the output waveform at jack $\overline{X}$ disappears.

r. Set TRUE-FALSE switches $\overline{K}$, $\overline{U}$ and $\overline{W}$ to TRUE. Observe that the output waveform at jack $\overline{X}$ disappears.

s. Set TRUE-FALSE switch $\overline{W}$ to FALSE. Observe that the waveform at jack $\overline{X}$ corresponds to the output waveform on figure 1.

t. Set TRUE-FALSE switches $\overline{W}$ to TRUE and $\overline{U}$ to FALSE. Observe that the waveform at jack $\overline{X}$ corresponds to the output waveform on figure 1.

u. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

v. Remove all jumper leads from the jacks.

w. Return all TRUE-FALSE switches to the neutral position.

x. Check for continuity between jacks $\overline{A}$, $\overline{B}$, and M.

y. Remove the card assembly from the test jack.

z. Return all switches and controls to the pretest position.

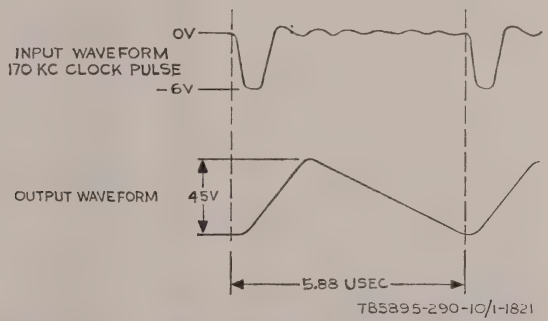


Figure 1. Write amplifier card assembly 530231, waveform diagram.

8. Read Amplifier Card Assembly 533094

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Press VOLTAGES switch 28 on.

b. Press SELECT switch 5 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 170.

e. Set the CLOCK PULSE VAR/−6V switch, to −6V.

f. Connect a jumper lead from jack Y to + DC VAR 1 and from jack $\overline{A}$ to SIGNALS CLOCK PULSE.

g. Adjust + DC VAR 1 for a 3-volt output.

h. Insert card assembly 533094 into test jack J1.

i. Press the ENERGIZE switch on.

j. Connect a jumper lead between jacks SIGNALS CLOCK PULSE and the input jacks in the sequence given in chart under *k* below.

k. Observe that the waveform at each output jack corresponds to the output waveform shown on figure 2.

Step No.	Input jack	Output jacks			
		Waveform A	Waveform B	Waveform C	Waveform D
1	E	C	V		
2	F			C	V
3	T	D	W		
4	U			D	W
5	$\overline{E}$	$\overline{V}$	$\overline{C}$		
6	$\overline{F}$			$\overline{V}$	$\overline{C}$
7	$\overline{T}$	$\overline{W}$	$\overline{D}$		
8	$\overline{U}$			$\overline{W}$	$\overline{D}$

l. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

m. Remove all jumper leads from the jacks.

n. Return all TRUE-FALSE switches to the neutral position.

o. Remove the card assembly from the test jack.

p. Return all switches and controls to the pretest positions.

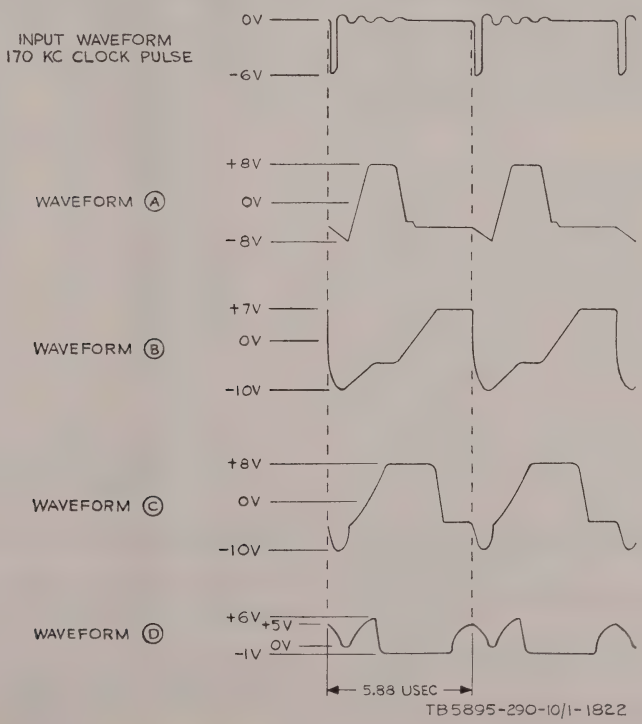


Figure 2. Read amplifier card assembly 533094, waveform diagram.

9. Gate Amplifier Card Assembly 534001

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Press VOLTAGES switches −7.5, −28, and 28 on.

b. Press SELECT switches 7 and 5 on.

c. Set TRUE-FALSE switches $\overline{B}$ to FALSE, and M to TRUE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 170.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

f. Press the RANDOM WORD GENERATOR switches for any word combination, and press the SPECIAL WORD ON switch on.

g. Connect a jumper lead from the SIGNALS WORD jack to the input jacks in sequence, and connect LOAD between the output jacks and GRD in the sequence given in chart under *j* below. Set the LOAD 1 switch to position 3.

h. Insert card assembly 534001 into test jack J1.

i. Press the ENERGIZE switch on.

j. Read the word at each output when connected, in turn, to the load as shown in the following chart.

Step No.	Input	Output
1	C	F, H
2	$\overline{C}$	$\overline{F}$, $\overline{H}$
3	D	J, K, L
4	$\overline{D}$	$\overline{J}$, $\overline{K}$, $\overline{L}$
5	E	J, K, L
6	$\overline{E}$	$\overline{J}$, $\overline{K}$, $\overline{L}$
7	U	N, P, R
8	$\overline{U}$	$\overline{N}$, $\overline{P}$, $\overline{R}$
9	V	N, P, R
10	$\overline{V}$	$\overline{N}$, $\overline{P}$, $\overline{R}$
11	W	S, T
12	$\overline{W}$	$\overline{S}$, $\overline{T}$

k. Press the −DC VAR 1 switch on.

l. Adjust the DC VAR 1 control for a −1 volt output.

m. Remove the jumper lead from the SIGNALS WORD jack.

n. Connect the jumper lead from DC VAR 1 to the input jacks, in turn, as given in the chart under *j* above.

o. Connect LOAD 1 between GRD and the outputs indicated in the chart under *j* above. Set the LOAD 1 switch to position 3.

p. Measure −1 volt at each output when connected, in turn, to the load as shown in the chart under *j* above.

q. Adjust DC VAR 1 for a −40 volt output.

r. Repeat the steps given in *n*, *o*, and *p* above. Measure −6 volts at the outputs indicated.

s. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

t. Remove all jumper leads from the jacks.

u. Return all TRUE-FALSE switches to the neutral position.

v. Remove the card assembly from the test jack.

w. Return all switches and controls to pretest positions.

10. Logic Converter Card Assembly 534393

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Press VOLTAGES switches 1.5 and −28 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Connect a jumper lead from jack $\overline{M}$ to DC VOLTAGES −12.

e. Insert card assembly 534393 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		T		
	1	t	W	−12
	2	f	W	0
II		$\overline{R}$		
	1	t	$\overline{C}$	−12
	2	f	$\overline{C}$	0

h. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

i. Return all TRUE-FALSE switches to the neutral position.

j. Measure 0 ohm between jacks J and $\overline{R}$, and $\overline{M}$ and $\overline{N}$.

k. Remove the card assembly from the test jack.

11. 14-Core Shift Register Card Assembly 534770

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Press VOLTAGES switches 1.5 on.

b. Press SELECT switch 7 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 170.

e. Set the CLOCK PULSE AMPLITUDE switch to −6V.

f. Connect a jumper lead from jack $\overline{M}$ to DC VOLTAGES −15.

g. Insert card assembly 534770 into test jack J1.

h. Press the ENERGIZE switch on.

i. Press the SPECIAL 14 CORE REGISTER switch on.

j. Press the SPECIAL WORD ON switch on.

k. Synchronize the oscilloscope for a positive signal and connect to the SYNC WORD connector.

l. Connect jumper leads from jacks F to SPECIAL FR, J to SPECIAL JR, T to SPECIAL TR, and U to SPECIAL UR.

m. Press all of the RANDOM WORD GENERATOR switches for a true indication.

n. Observe that the output waveforms at TP1, TP2, TP3, and TP4, on card assembly, are 15 volt spikes riding at a −15 volt level.

o. Press the RANDOM WORD GENERATOR switch 1 to false.

p. Observe that the second spike at TP1, the third spike at TP2, the ninth spike at TP3, and the fourteenth spike at TP4 disappears.

q. Observe that when any RANDOM WORD GENERATOR switch is set false, the corresponding spike, which disappears, is delayed one time slot at TP1, two time slots at TP2, eight time slots at TP3, and 13 time slots at TP4.

r. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

s. Remove all jumper leads from the jacks.

t. Remove the card assembly from the test jack.

u. Return all TRUE-FALSE switches to the neutral positions.

v. Return all switches and controls to the pretest positions.

12. 6–8K Emitter Follower Card Assembly 534930

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Press VOLTAGES switches 50 and −7.5 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 170.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

f. Press the RANDOM WORD GENERATOR switches for a1010101010101000 word combination.

g. Press the SPECIAL WORD ON switch on.

h. Synchronize the oscilloscope for a negative signal and connect to the SYNC WORD jack.

i. Connect a jumper lead from the SIGNALS WORD jack to the input jacks, and connect a load between the output jacks and GRD in the sequence given in the chart under *l* below. Set the LOAD selector switch to position 2.

j. Insert card assembly 534930 into test jack J1.

k. Press the ENERGIZE switch on.

l. Read the word at each output jack when connected, in turn, to the load as shown in the following chart. Observe that the word at each output jack corresponds to the word at the input jack.

Step No.	Input jack	Output jack
1	J	D, E
2	K	F, H
3	L	N, P, R
4	S, T	U, V, W
5	$\overline{F}$, $\overline{H}$	$\overline{C}$, $\overline{D}$, $\overline{E}$
6	$\overline{N}$	$\overline{J}$, $\overline{K}$, $\overline{L}$
7	$\overline{P}$	$\overline{S}$, $\overline{T}$
8	$\overline{R}$	$\overline{U}$, $\overline{V}$

m. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

n. Remove all jumper leads from the jacks.

o. Remove the card assembly from the test jack.

p. Return all switches and controls to the pretest positions.

13. Servo Amplifier Card Assembly 539657

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches $\overline{B}$, F, and $\overline{T}$ to TRUE.

b. Connect a jumper lead from jack X to DC VOLTAGES −28.

c. Connect LOAD 1 and LOAD 2 in series and set the LOAD switches to position 2.

d. Connect a jumper lead from the end of one load to jack B. Connect a jumper lead from the end of the other load to jack D. Connect a jumper lead from the junction of the two loads to the DC VOLTAGES −28 jack.

e. Press the AC VAR switch on.

f. Synchronize the oscilloscope for a positive signal and connect to the SYNC SIGNAL connector.

g. Set the AC VAR FREQUENCY switch to VAR, and adjust the AC VAR FREQUENCY control for a 750-cps output.

h. Adjust the AC VAR AMPLITUDE control for a 0.5-volt output.

i. Connect a jumper lead from jack V to SIGNALS AC VARIABLE.

j. Insert card assembly 539657 into test jack J1.

k. Press the ENERGIZE switch on.

l. Observe that the waveform at jacks B and D correspond to waveform shown in figure 3.

m. Remove the jumper leads from jacks B and D, and connect the end of one load to jack $\overline{V}$ and the end of the other load to jack $\overline{X}$.

n. Remove the jumper lead from jack V, and connect to jack $\overline{D}$.

o. Observe that the waveform on jacks $\overline{X}$ and $\overline{V}$ correspond to waveform shown in figure 3.

p. Press the ENERGIZE switch off.

q. Remove all jumper leads from the jacks.

r. Return all TRUE-FALSE switches to the neutral positions.

s. Return all switches and controls to the pretest positions.

t. Measure 0 ohm between the jacks and test points listed below.

TPB1–2 and B
TPB1–6 and D
TPB1–4 and $\overline{X}$
TPB1–8 and $\overline{V}$
$\overline{B}$ and $\overline{C}$

u. Remove the card assembly from the test jack.

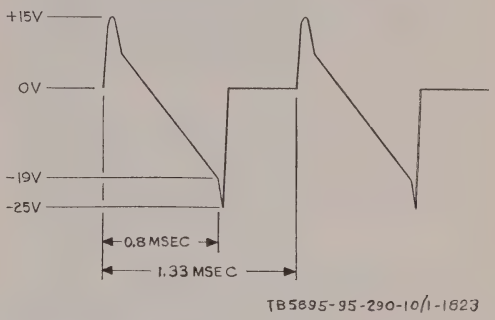


Figure 3. Servo amplifier card assembly 539657, waveform diagram.

14. Emitter Follower Card Assembly 539818

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switch −28 on.

b. Press SELECT switch 5 on.

c. Set TRUE-FALSE switches M, N, and $\overline{C}$ to TRUE.

d. Set the AC VAR FREQUENCY switch to 1KC.

e. Adjust the AC VAR AMPLITUDE control for a 2-volt output.

f. Connect jumper leads from the SIGNALS AC VARIABLE jack to the input jacks and connect LOAD 1 between the output jacks and GRD in the sequence given in the chart under *i* below, and set the LOAD 1 selector switch to position 4.

g. Insert card assembly 539818 into test jack J1.

h. Press the ENERGIZE switch on.

i. Observe that the sine wave at each output jack is 1.8 volts or greater.

Step No.	Input jacks	Output jacks
1	C	$\overline{D}$
2	J	$\overline{L}$
3	W	$\overline{X}$
4	$\overline{K}$	$\overline{R}$
5	R	$\overline{S}$
6	$\overline{W}$	Z

j. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

k. Remove all jumper leads from the jacks.

l. Remove the card assembly from the test jack.

m. Return all TRUE-FALSE switches to the neutral positions.

n. Return all switches and controls to the pretest positions.

15. Trigger Gate Card Assembly 539857

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switches −7.5, and 50 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches M and $\overline{F}$ to TRUE.

d. Connect a load between jacks B and L, and set the LOAD switch to position 2.

e. Insert card assembly 539857 into test jack.

f. Press the ENERGIZE switch on.

g. Set TRUE-FALSE switches B and $\overline{C}$ to FALSE.

h. Measure 0 volt at jack N.

i. Set TRUE-FALSE switch B to TRUE.

j. Measure −6 volts at jack N.

k. Set TRUE-FALSE switch $\overline{C}$ to TRUE.

l. Measure 0 volt at jack N.

m. Set TRUE-FALSE switch B to FALSE.

n. Measure 0 volt at jack N.

o. Set TRUE-FALSE switch $\overline{C}$ to FALSE and $\overline{F}$ to neutral.

p. Measure −6 volts at jack N.

q. Set TRUE-FALSE switches $\overline{F}$, B, $\overline{P}$ to TRUE.

r. Measure 0 volt at jack N.

s. Set TRUE-FALSE switch $\overline{P}$ to FALSE.

t. Measure −6 volts at jack N.

u. Return $\overline{P}$ to neutral.

v. Repeat step *d* and steps *g* through *u*, above, substituting jacks D, $\overline{V}$, $\overline{W}$, and $\overline{T}$ for jack L and jacks P, $\overline{A}$, $\overline{L}$, and $\overline{N}$ for jack N.

w. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

x. Remove all jumper leads from the jacks.

y. Return all TRUE-FALSE switches to their neutral positions.

z. Measure 287 ohms between jacks $\overline{X}$ and $\overline{F}$ (connect + lead of meter to jack $\overline{F}$).

aa. Remove the card assembly from the test jacks.

16. Matrix Card Assembly 54
(fig. 4)

a. Set TRUE-FALSE switche
M, N, P, R, S, U, W, X, Y, Z,
to FALSE.

b. Press VOLTAGES switches

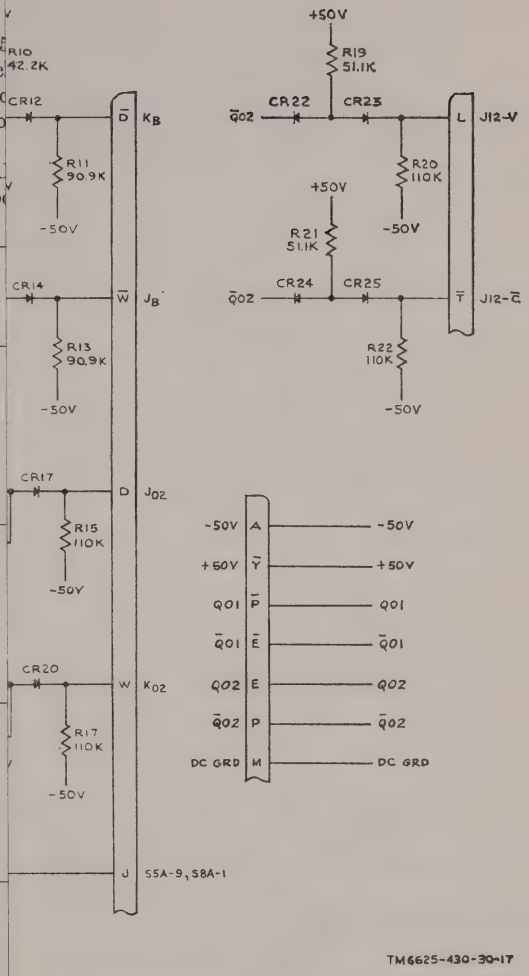
c. Press SELECT switch 1 on.

d. Insert matrix assembly 5405

e. Press the ENERGIZE switc

f. Make TRUE-FALSE switc
sequence given in the chart belo
Check the output logic voltages
indicated. Return the TRUE-FA
in each test to FALSE before pro
test.

Test No.	Step No.	TRUE-FALSE switches			
I		F	P	Z	$\overline{A}$
	1	t	t	t	t
	2	f	t	t	t
	3	t	f	t	t
	4	t	t	f	t
	5	t	t	t	f
II		J	R	Z	$\overline{A}$
	1	t	t	t	t
	2	f	t	t	t
	3	t	f	t	t
	4	t	t	f	t
	5	t	t	t	f
III		N	U	Z	$\overline{A}$
	1	t	t	t	t
	2	f	t	t	t
	3	t	f	t	t
	4	t	t	f	t
	5	t	t	t	f
IV		L	Z	$\overline{A}$	$\overline{F}$
	1	t	t	t	t
	2	f	t	t	t
	3	t	f	t	t
	4	t	t	f	t
	5	t	t	t	f



TM6625-430-30-17

mbly 540551, schematic diagram.

16. Matrix Card Assembly 540551

(fig. 4)

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, U, W, X, Y, Z, $\overline{A}$, $\overline{F}$, $\overline{J}$, $\overline{N}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 540551 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F P Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		J R Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		N U Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		L Z $\overline{A}$ $\overline{F}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		M Z $\overline{A}$ $\overline{J}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		W Z $\overline{A}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		X Z $\overline{A}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		H Y Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		K S Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

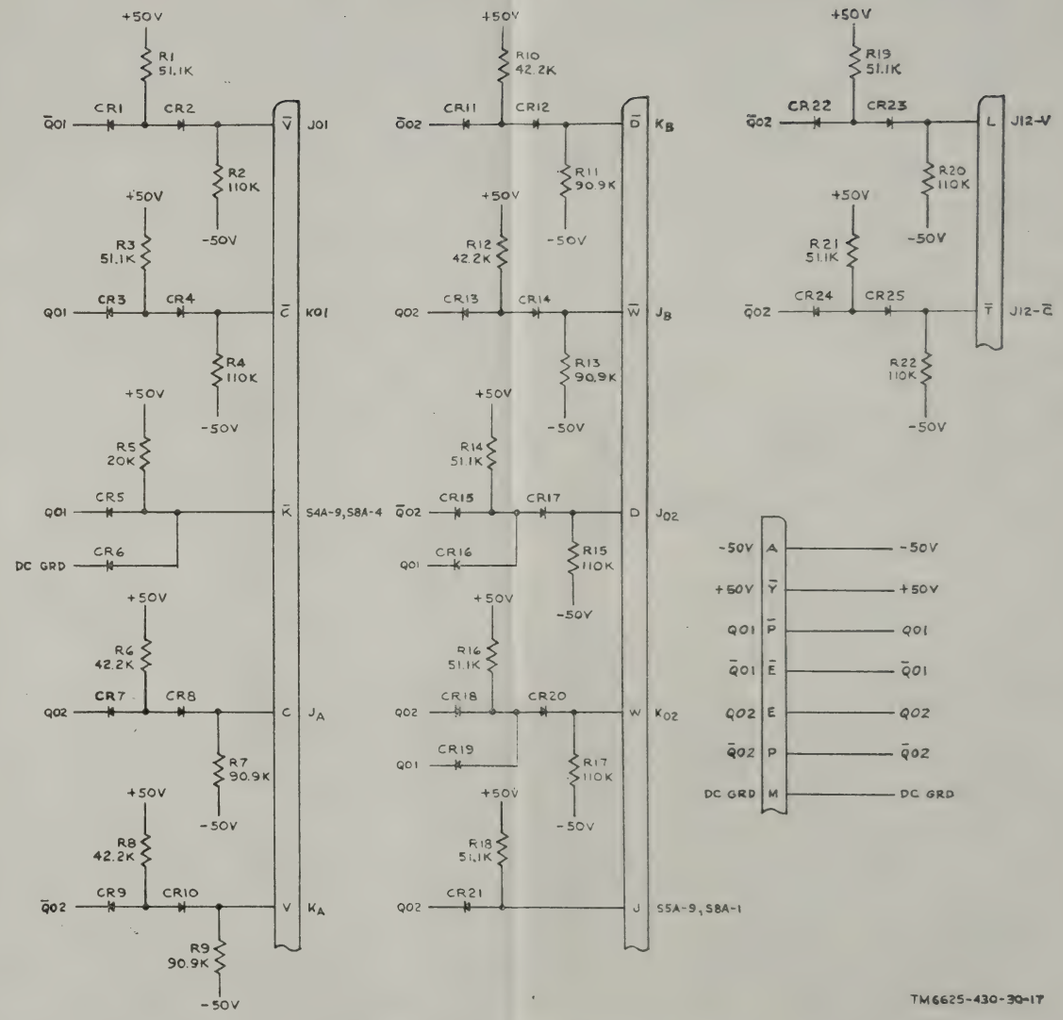
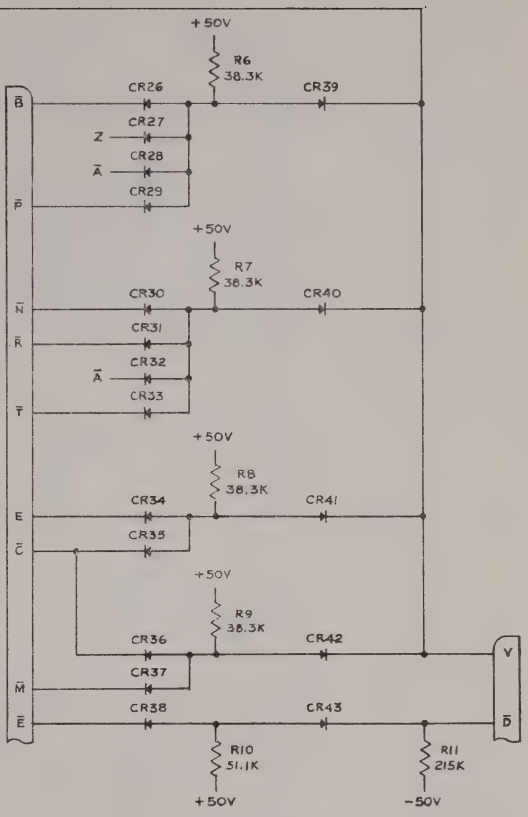


Figure 4. Matrix card assembly 540551, schematic diagram.

17. M

a. Se
U, X, Y
FALSE
b. Pr
c. Pr
d. C
DC VO
LOAD
e. In
f. Pr
g. M
sequenc
Check
indicat
in each
test.

Test No.	S
I	
II	
III	
IV	



NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE HD2270.

TM6625-429-24-19

trix card assembly 540553, schematic diagram.

17. Matrix Card Assembly 540553

(fig. 5)

a. Set TRUE-FALSE switches E, K, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{H}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a load in series between jacks V and DC VOLTAGES −50 with jumper leads, and set LOAD switch to position 8.

e. Insert matrix assembly 540553 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{E}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
II		K R Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		P S Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		T U Z $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		X Z $\overline{A}$ $\overline{H}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		Y Z $\overline{A}$ $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		Z $\overline{A}$ $\overline{B}$ $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		$\overline{A}$ $\overline{N}$ $\overline{R}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		E $\overline{C}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
X		$\overline{C}$ $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

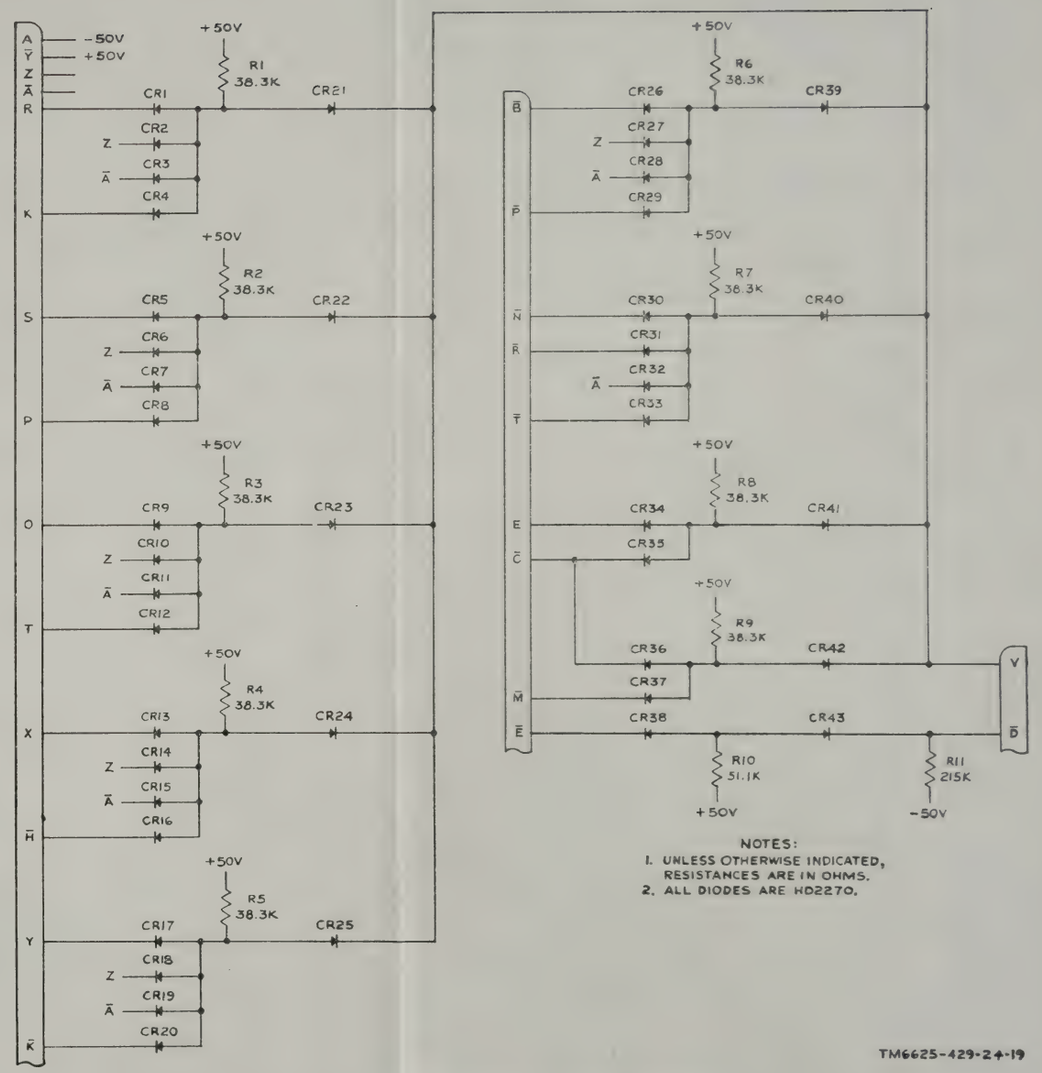
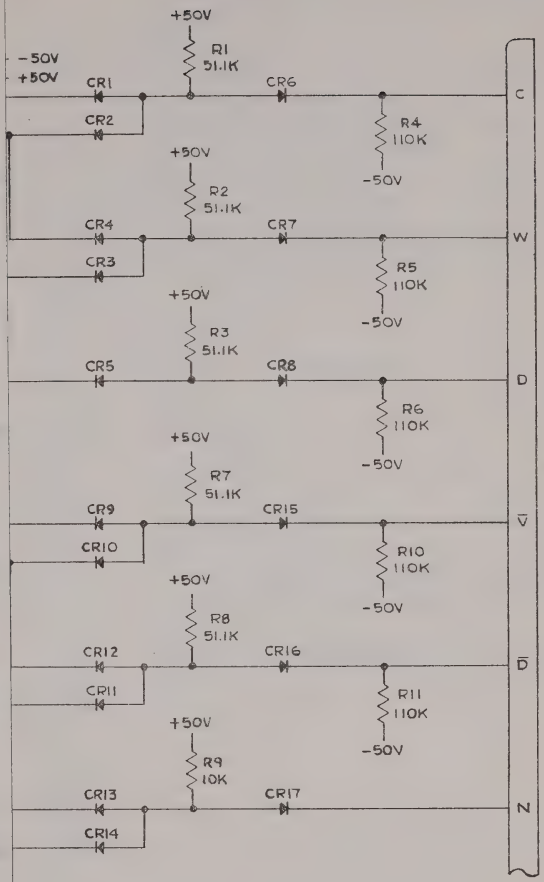


Figure 5. Matrix card assembly 540553, schematic diagram.



NOTES:
1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE HD2270.

TM6625-429-24-21

Figure 6. Matrix card assembly 540555, schematic diagram.

Assembly 210233

18. Matrix Card Assembly 540555

(fig. 6)

a. Set TRUE-FALSE switches M, $\overline{E}$, $\overline{F}$, $\overline{L}$, $\overline{M}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a load in series between jacks N and DC VOLTAGES −50 with jumper leads, and set LOAD switch to position 8.

e. Insert matrix assembly 540555 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

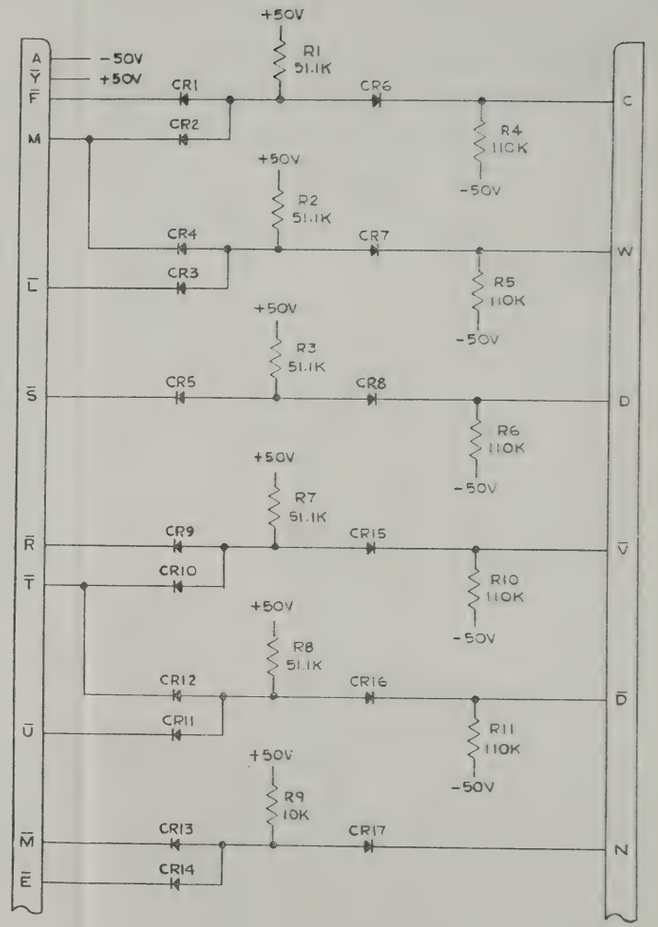
Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		M $\overline{F}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		M $\overline{L}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
III		$\overline{R}$ $\overline{T}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		$\overline{E}$ $\overline{M}$		
	1	t t	N	0
	2	f t	N	−6
	3	t f	N	−6
V		$\overline{T}$ $\overline{U}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		$\overline{S}$		
	1	t	D	0
	2	f	D	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.



NOTES:
1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE HD2270.

TM6625-429-24-21

Figure 6. Matrix card assembly 540555, schematic diagram.

19. Matrix Card Assembly 5

(fig. 7)

a. Set TRUE-FALSE switche
M, N, P, R, S, X, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$
and $\overline{S}$ to FALSE.

b. Press VOLTAGES switche

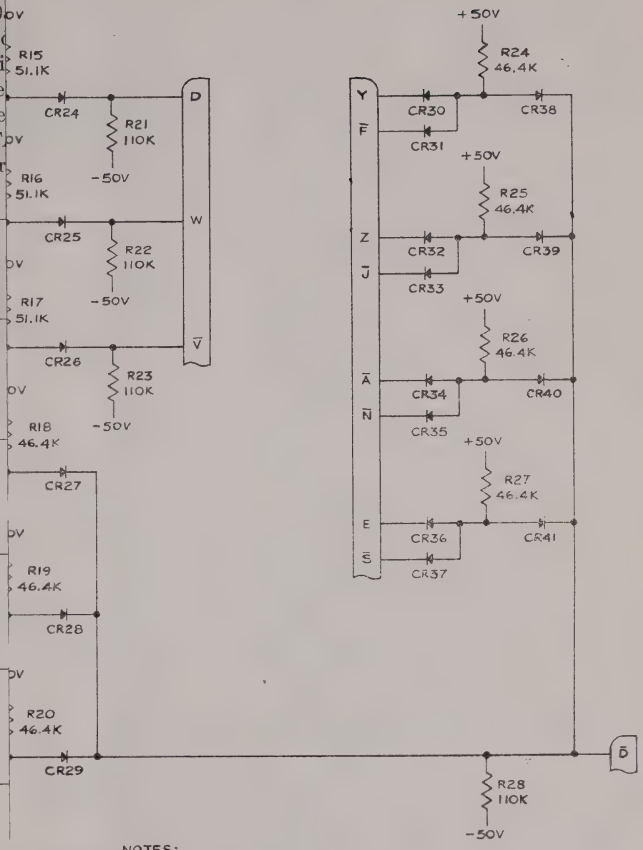
c. Press SELECT switch 1 or

d. Insert matrix assembly 540

e. Press ENERGIZE switch

f. Make TRUE-FALSE swi
sequence given in the chart be
Check the output logic voltage
indicated. Return the TRUE-F
in each test to FALSE before pr
test.

Test No.	Step No.	TRUE-FALSE switches
I		J L
	1	t t
	2	f t
	3	t f
II		$\overline{N}$ $\overline{X}$
	1	t t
	2	f t
	3	t f
III		M S
	1	t t
	2	f t
	3	t f
IV		Y $\overline{F}$
	1	t t
	2	f t
	3	t f
V		Z $\overline{J}$
	1	t t
	2	f t
	3	t f
VI		$\overline{A}$ $\overline{N}$
	1	t t
	2	f t
	3	t f
VII		E $\overline{S}$
	1	t t
	2	f t
	3	t f



NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE HD2270.

TM6625-429-24-23

...bly 540557, schematic diagram.

19. Matrix Card Assembly 540557

(fig. 7)

a. Set TRUE-FALSE switches E, F, H, J, K, L, M, N, P, R, S, X, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 540557 into test jack J1.

e. Press ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J L		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
II		$\overline{N}$ $\overline{X}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−8
III		M S		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		Y $\overline{F}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
V		Z $\overline{J}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		$\overline{A}$ $\overline{N}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		E $\overline{S}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		$\overline{R}$		
	1	t	D	0
	2	f	D	−6
IX		F		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
X		$\overline{K}$		
	1	t	W	0
	2	f	W	−6
XI		$\overline{E}$		
	1	t	U	0
	2	f	U	−6
XII		K		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XIII		P		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
XIV		$\overline{P}$		
	1	t	C	0
	2	f	C	−6
XV		$\overline{H}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XVI		H		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XVII		R		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Remove the matrix assembly from the test jack.

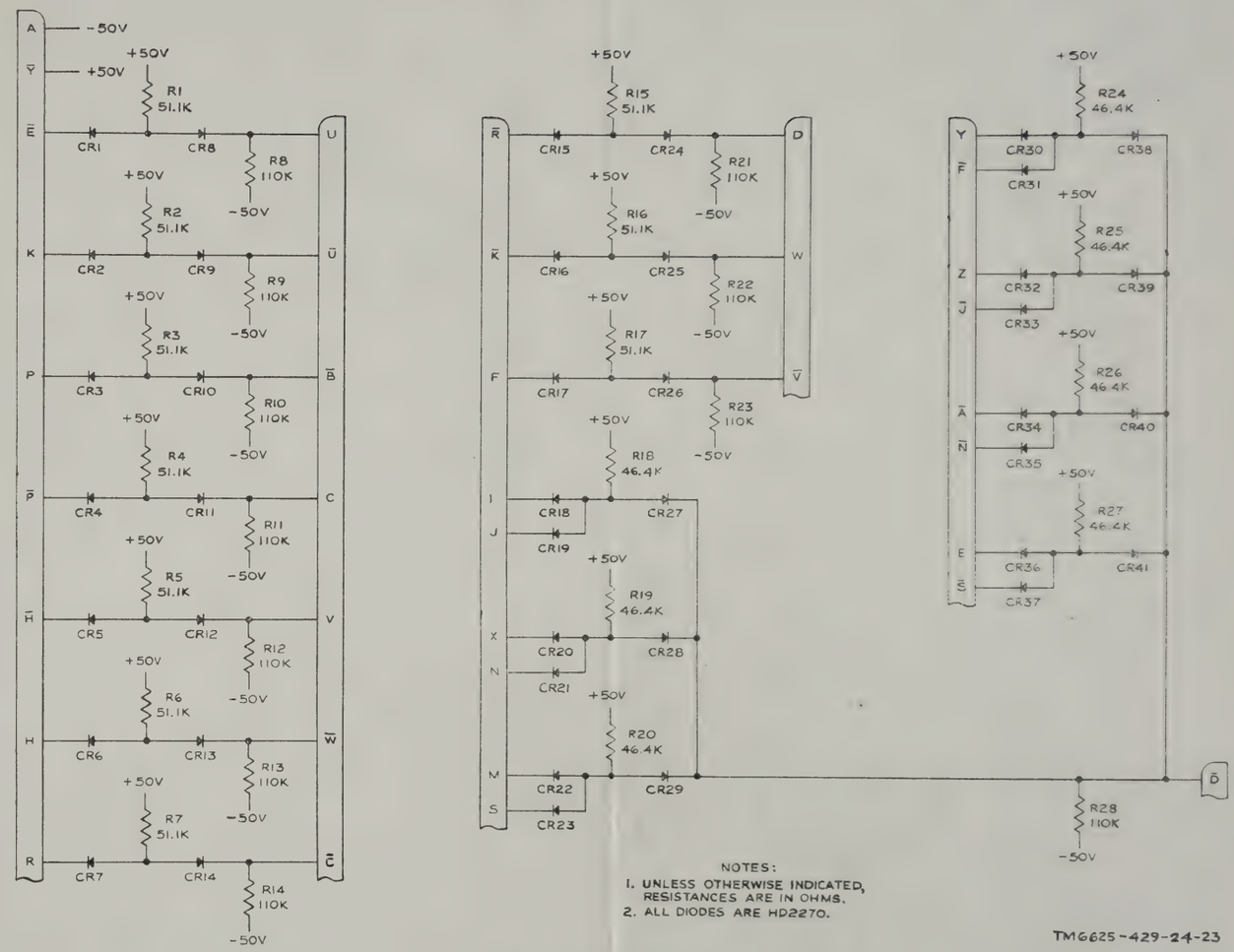
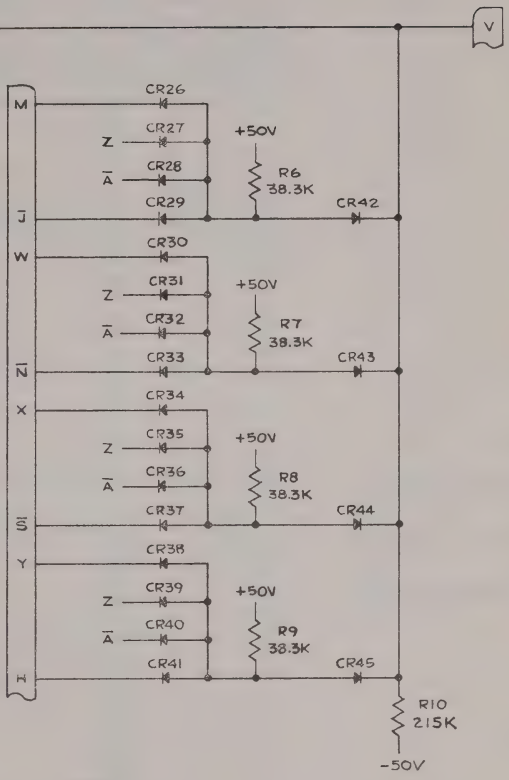


Figure 7. Matrix card assembly 540557, schematic diagram.

20. M

a. S
P to F
b. P
c. P
d. I
e. P
f. M
sequen
Check
indicat
in each
test.

Test No.	S
I	
II	
III	



NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE HD2270.

TM6625-429-24-17

trix card assembly 540848, schematic diagram.

20. Matrix Card Assembly 540848

(fig. 8)

a. Set TRUE-FALSE switches E, M, P, $\overline{E}$, and $\overline{P}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 540848 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{E}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
II		$\overline{P}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
III		M $\overline{P}$		
	1	t t	$\overline{K}$	0
	2	f t	$\overline{K}$	−6
	3	t f	$\overline{K}$	−6
IV		E		
	1	t	C, J, $\overline{W}$	0
	2	f	C, J, $\overline{W}$	−6
V		P		
	1	t	L, V, $\overline{D}$, $\overline{T}$	0
	2	f	L, V, $\overline{D}$, $\overline{T}$	−6
VI		P $\overline{P}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		E $\overline{P}$		
	1	t t	$\overline{W}$	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

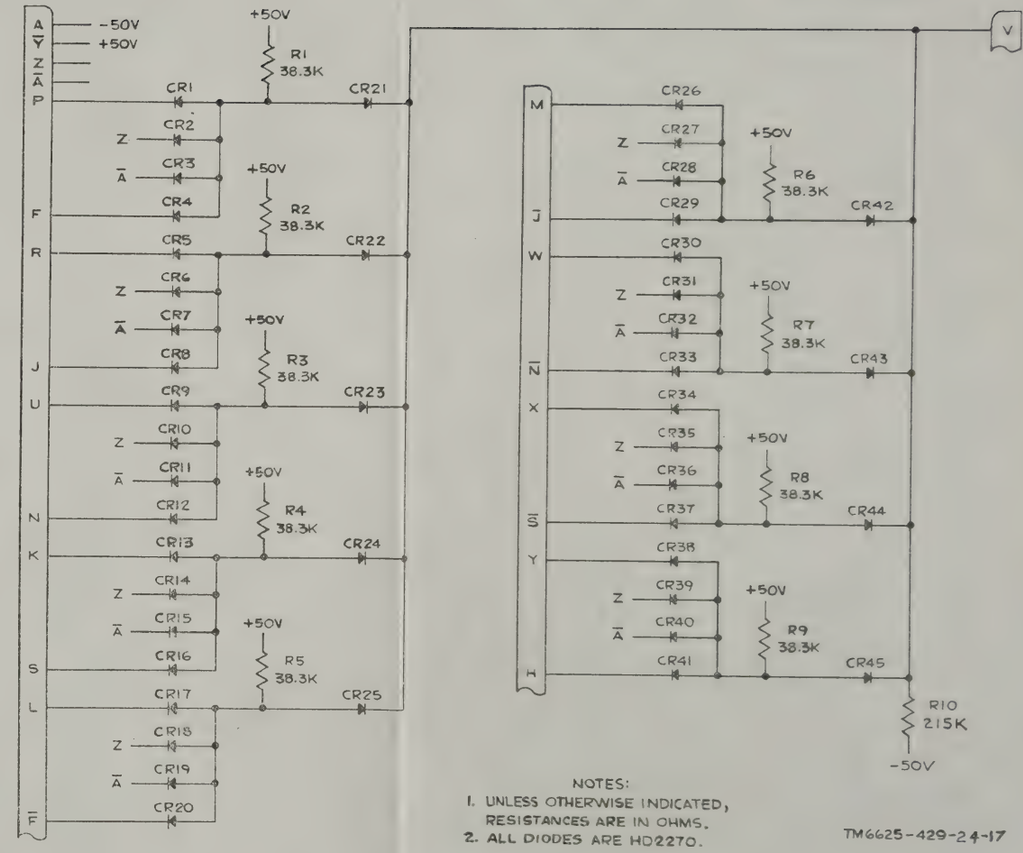


Figure 8. Matrix card assembly 540848, schematic diagram.

21. Blocking Oscillator Card Assembly 542303 (fig. 9)

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Press VOLTAGES switches 1.5, −7.5, and 28 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Press the CLOCK PULSE switch on.

e. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

f. Set the CLOCK PULSE FREQUENCY KC selector switch to 50.

g. Set the CLOCK PULSE AMPLITUDE switch to −6V.

h. Connect a jumper lead from jack H to SIGNALS CLOCK PULSE.

i. Insert card assembly 542303 into test jack J1.

j. Press the ENERGIZE switch on.

k. Observe that the waveforms at jack N and TP1B on the card assembly correspond with waveform A.

l. Remove the jumper lead from jack H and connect to jack $\overline{U}$.

m. Observe that the waveforms at jack Y and TP3B on the card assembly correspond with waveform A.

n. Remove the jumper lead from jack $\overline{U}$ and connect to jack B.

o. Observe that the waveforms at jack $\overline{A}$ and TP2B on the card assembly correspond with waveform A.

p. Observe that the waveforms at jack A and TP4B on the card assembly correspond with waveform B.

q. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

r. Remove all jumper leads from the jacks.

s. Remove the card assembly from the test jack.

t. Return all switches and controls to the pretest positions

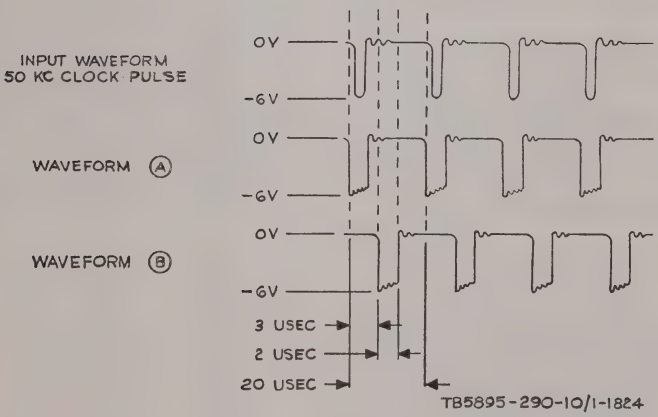
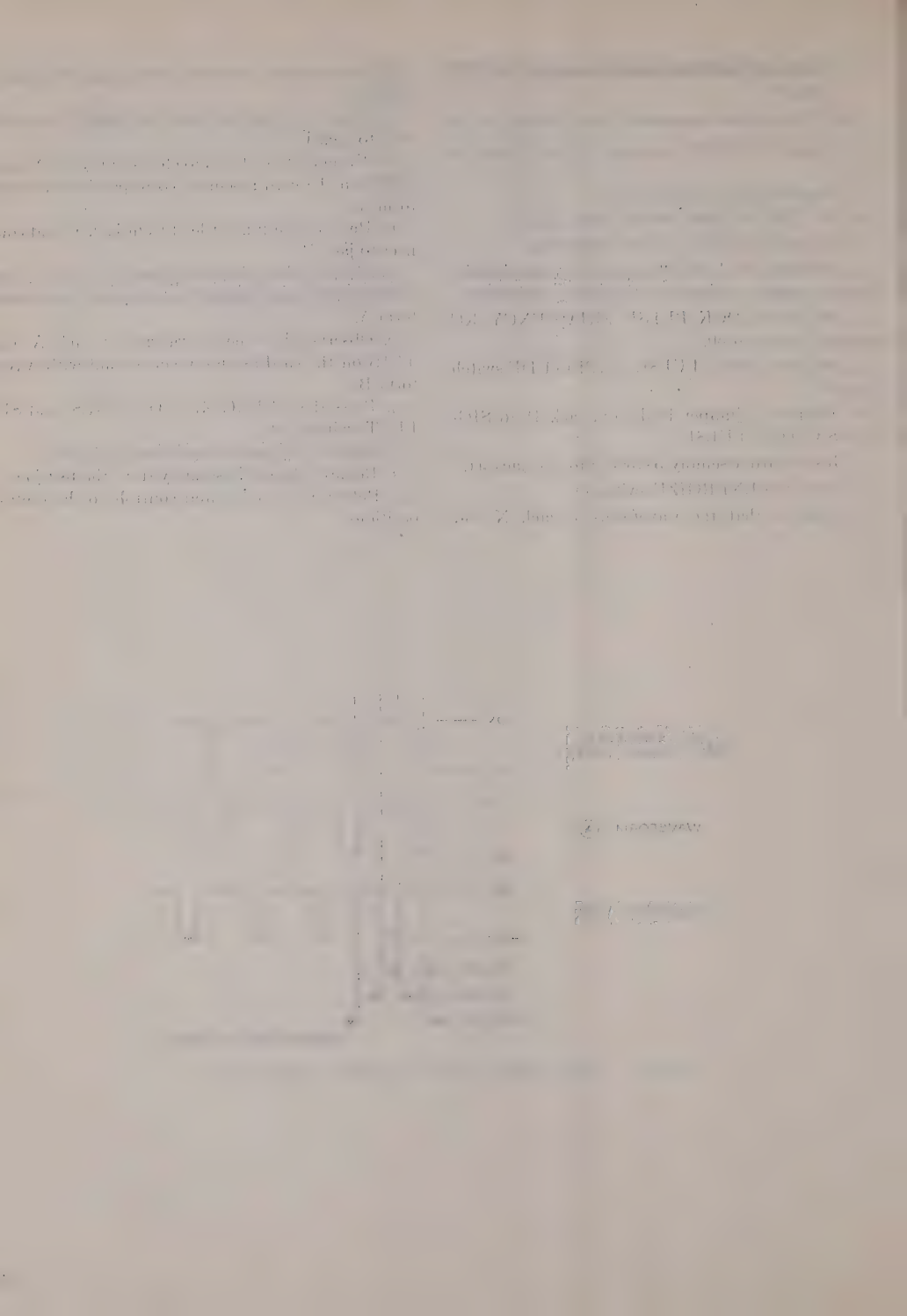


Figure 9. Blocking oscillator card assembly 542303, waveform diagram.



22. Sweep Switch Card Assembly 543928

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches M to TRUE and $\overline{B}$ and $\overline{H}$ to FALSE.

b. Set the AC VAR FREQUENCY switch to 1KC.

c. Press the REF PULSE switch on.

d. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

e. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a 6-volt output.

f. Set the REF PULSE DURATION control to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

g. Connect LOAD 1 between jacks $\overline{W}$ and DC VOLTAGES 28 with jumper leads, and set the LOAD 1 selector switch to position 5.

h. Set DELAY ADJ controls R1, R3, R5, R7, R9, R11, R13, R15, R17, R19, and R21 on the card assembly to the mid range positions.

i. Insert card assembly 543928 into test jack J1.

j. Press the ENERGIZE switch on.

k. Connect a jumper lead from SIGNALS REF PULSE to the input jacks, and connect LOAD 2 between the output jacks and DC VOLTAGES 12 in the sequence given in the chart under *l* below. Set the LOAD 2 selector switch to position 4.

l. Set TRUE-FALSE switch $\overline{H}$ to FALSE for each step. Observe −5 volt to 12 volt positive going pulses, 500 μsec in duration, adjust the DELAY ADJ controls and note variations of trigger delay time from 0 to over 1 μsec at each output jack.

Step	Input jack	Output jack	DELAY ADJ potentiometer
1	F	E	R1
2	K	J	R3
3	P	N	R5
4	S	R	R7
5	U	T	R9
6	$\overline{D}$	$\overline{C}$	R11
7	$\overline{F}$	$\overline{E}$	R13
8	$\overline{K}$	$\overline{J}$	R15
9	$\overline{P}$	$\overline{N}$	R17
10	$\overline{S}$	$\overline{R}$	R19

m. Remove jumper lead from jack $\overline{S}$ and connect to jack $\overline{T}$.

n. At jack $\overline{W}$ observe −4volt to 28 volt positive pulses 500 μsec. in duration.

o. Observe that the adjustment of DELAY ADJ control R21 varies the trigger delay time of the waveform at jack $\overline{W}$ from 0 to 1 μsec.

p. Press the ENERGIZE switch off.

q. Remove all jumper leads from the jacks.

r. Return all TRUE-FALSE switches to the neutral positions.

s. Return all switches and controls to the pretest positions.

t. Remove the card assembly from the test jack.

23. Digilog Switch Card Assembly 543929

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Press VOLTAGES switches 1.5 and 28 on.

b. Press SELECT switches 7, 4, and 3 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Set the AC VAR FREQUENCY switch to 1KC.

e. Press the REF PULSE switch on.

f. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

g. Set the REP PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −8-volt output.

h. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

i. Connect a jumper lead from jack X to DC VOLTAGES 8.

j. Connect a 1,000-ohm, 1-watt resistor in series with a 4,700-ohm 1-watt resistor between jacks DC VOLTAGES 8 and SIGNALS REF PULSE. (Connect the 1,000-ohm resistor to SIGNALS REF PULSE and the 4,700 ohm resistor to DC VOLTAGES 8.) Connect a jumper lead from the junction of the two resistors to each input jack in the sequence given in the chart under *n* below.

k. Connect a load between each output jack and GRD with jumper leads, and set the LOAD selector switch to position 3.

l. Insert card assembly 543929 into test jack J1.

m. Press the ENERGIZE switch on.

n. Observe at each output jack, when connected

to the load, 0 to 4 volt positive going pulses, 500 μsec in duration. Note in test 12, the output at jack T is the same as the input, only inverted.

Test	Input jack	Output jack	Waveform
1	A	B	A
2	E	F	A
3	J	K	A
4	N	P	A
5	R	S	A
6	T	U	A
7	$\overline{C}$	$\overline{D}$	A
8	$\overline{E}$	$\overline{F}$	A
9	J	$\overline{K}$	A
10	$\overline{N}$	$\overline{P}$	A
11	$\overline{R}$	$\overline{S}$	A
12	$\overline{W}$	$\overline{T}$	B

o. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

p. Remove all jumper leads from the jacks.

q. Remove the card assembly from the test jack.

r. Return all TRUE-FALSE switches to the neutral positions.

s. Return all switches and controls to the pretest positions.

24. Digilog Resistor Network Card Assembly 544592

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Insert card assembly 544592 into test jack.

b. Measure 20,000 ohms between the following jacks:

F and K
K and P
P and S
S and U
U and $\overline{D}$
$\overline{D}$ and $\overline{F}$
$\overline{F}$ and $\overline{K}$
$\overline{K}$ and $\overline{P}$
$\overline{P}$ and $\overline{S}$

c. Measure 16,000 ohms between jacks B and F.

d. Measure 46,000 ohms between jacks F and $\overline{W}$.

e. Measure 22,000 ohms between jacks D and $\overline{T}$.

f. Measure 6,000 ohms between jacks $\overline{T}$ and $\overline{W}$.

g. Measure 16,000 ohms between jacks $\overline{S}$ and $\overline{T}$.

h. Measure 0 ohm between jacks M and GRD and $\overline{W}$ and $\overline{L}$.

i. Remove the card assembly from the test jack.

25. Digit Square Wave Generator Card Assembly 546643

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Press VOLTAGES switches −28 and 28 on.

b. Press SELECT switch 5 on.

c. Set TRUE-FALSE switches M to TRUE, and $\overline{B}$ to FALSE.

d. Press the CLOCK PULSE switch on.

e. Set the CLOCK PULSE AMPLITUDE switch to −6V. Set the CLOCK PULSE FREQUENCY KC switch to 170.

f. Synchronize oscilloscope for a negative signal and connect to the SYNC SIGNAL jack.

g. Connect a jumper lead from jack $\overline{V}$ to SIGNALS DSW.

h. Insert card assembly 546643 into test jack J1.

i. Press the ENERGIZE switch on.

j. Observe that the waveform at jacks C, $\overline{W}$, and TP7 is a −6-volt, 170-kc square wave.

k. Observe that the waveform at test points TP3 and TP5, on card assembly is a −8 to −14-volt, 170-kc square wave.

l. Observe that the waveform at jacks W, $\overline{C}$, and TP8 is the inverse of waveform at jacks C and $\overline{W}$.

m. Observe that the waveform at test points TP1 and TP2, on card assembly is a −8 to −14-volt, 170-kc square wave.

n. Observe that the waveform at test point TP4, on card assembly, is a −6 to −9-volt, 170-kc square wave.

o. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

p. Remove all jumper leads from the jacks.

q. Remove the card assembly from the test jack.

r. Return all switches and controls to the pretest positions.

26. Amplifier Card Assembly 546804

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Press VOLTAGES switch −28 on.

b. Press SELECT switch 8 on.

c. Set TRUE-FALSE switches C, P, T, $\overline{A}$, $\overline{D}$, $\overline{K}$, and $\overline{W}$ to TRUE.

d. Set the AC VAR FREQUENCY switch to 1KC, and adjust the AC VAR AMPLITUDE control for a 0.5 volt output.

e. Connect jumper leads from jacks S, $\overline{F}$, and $\overline{Y}$ to SIGNALS AC VARIABLE.

f. Connect a load between jack $\overline{H}$ and GRD with jumper leads, and set the LOAD selector switch to position 3.

g. Set the AMPL NO.—GAIN controls R4, R16, and R28, on card assembly, fully clockwise.

h. Insert card assembly 546804 into test jack J1.

i. Press the ENERGIZE switch on.

j. Readjust the AC VAR AMPLITUDE control for a 0.5 volt output.

k. Measure −28 volts at TP1 on card assembly.

l. Observe a 0.5 volt sine wave at TP5, a 0.25 volt sine wave at jack $\overline{X}$ and TP6, a 13 volt sine wave at jack $\overline{H}$ and TP4, and 6.5 volt sine wave at jack $\overline{J}$ and TP3.

m. Adjust the AMPL NO.—GAIN control R4, on card assembly, counterclockwise and observe that the voltage at jack $\overline{H}$ and TP4 decreases.

n. Remove the jumper lead from jack $\overline{H}$ and connect to jack V.

o. Observe a 0.5 volt sine wave at TP11, a 0.25 volt sine wave at jack $\overline{E}$ and TP12, a 13 volt sine wave at jack V and TP10, and a 6.5 volt sine wave at jack U and TP9.

p. Adjust AMPL NO.—GAIN control R16, on card assembly, counterclockwise and observe that the voltage at jack V and TP10 decreases.

q. Remove the jumper lead from jack V and connect to jack A.

r. Observe a 0.5 volt sine wave at TP17, a 0.25 volt sine wave at jack R and TP18, a 13-volt sine wave at jack A and TP16, and a 6.5 volt sine wave at jack B and TP15.

s. Adjust the AMPL NO.—GAIN control R28, on card assembly, counterclockwise and observe that the voltage at jack A and TP16 decreases.

t. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

u. Remove all jumper leads from the jacks.

v. Return all TRUE-FALSE switches to the neutral positions.

w. Remove the card assembly from the test jack.

x. Return all switches and controls to the pretest positions.

27. Hybrid Network Card Assembly 546806

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Insert card assembly 546806 into test jack J1.

b. Measure 732 ohms between the jacks as marked below.

From	To
A	R T W
B	S U V
C	N U W
D	P T V
E	P S W
F	N R V
H	P R U
J	N S T
$\overline{A}$	$\overline{R}$ T W
$\overline{B}$	$\overline{S}$ $\overline{U}$ $\overline{V}$
$\overline{C}$	$\overline{N}$ $\overline{U}$ $\overline{W}$
$\overline{D}$	P $\overline{T}$ $\overline{V}$
$\overline{E}$	P $\overline{S}$ $\overline{W}$
$\overline{F}$	$\overline{N}$ $\overline{R}$ $\overline{V}$
$\overline{H}$	P $\overline{R}$ $\overline{U}$
$\overline{J}$	$\overline{N}$ $\overline{S}$ $\overline{T}$

c. Remove the card assembly from the test jack.

28. Fast Flip-flop Card As
(fig. 10)

Note. The schematic diagram is
and TM 11–5840–272–30/19.

a. Press VOLTAGES swi
and 28 on.

b. Press SELECT switches

c. Set TRUE-FALSE sw
and $\overline{B}$ to FALSE.

d. Set the CLOCK PULS
selector switch to 524.

e. Set the CLOCK PUL
to −6V.

f. Insert card assembly 54

g. Press the ENERGIZE s

h. Use the jumper leads
between the column 1 jacks,
chart under *j* below, and se
to position 1. Connect LOAD
2 jacks, in turn, as listed in t
and set LOAD 2 switch to po

i. Connect jumper leads
CLOCK PULSE jacks to th
as indicated in the chart und

j. Observe that the wavef
indicated in the chart below
forms shown in figure 10.

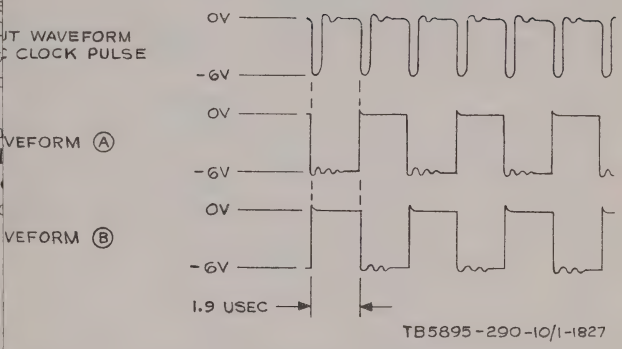


Figure 10. Fast flip-flop card assembly 547514, waveform diagram.

28. Fast Flip-flop Card Assembly 547514

(fig. 10)

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Press VOLTAGES switches 1.5, −7.5, −28, and 28 on.

b. Press SELECT switches 7 and 5 on.

c. Set TRUE-FALSE switches M to TRUE- and $\overline{B}$ to FALSE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 524.

e. Set the CLOCK PULSE VAR −6V switch to −6V.

f. Insert card assembly 547514 into test jack J1.

g. Press the ENERGIZE switch on.

h. Use the jumper leads to connect LOAD 1 between the column 1 jacks, in turn, as listed in the chart under *j* below, and set the LOAD 1 switch to position 1. Connect LOAD 2 between the column 2 jacks, in turn, as listed in the chart under *j* below, and set LOAD 2 switch to position 1.

i. Connect jumper leads from the SIGNALS CLOCK PULSE jacks to the input jacks, in turn, as indicated in the chart under *j* below.

j. Observe that the waveforms at the test points indicated in the chart below correspond to the waveforms shown in figure 10.

Step No.	Load connection jacks		Input jacks	Test points	Waveform
	Column 1	Column 2			
1	C and P	E and V	$\overline{L}$ and $\overline{N}$	F, H, J, K	A
				R, S, T, U	B
2	D and P	E and W	N and $\overline{A}$	F	A
				R	B
3	$\overline{D}$ and $\overline{P}$	$\overline{E}$ and $\overline{W}$	$\overline{L}$ and $\overline{N}$	$\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$	A
				$\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$	B
4	$\overline{C}$ and $\overline{P}$	$\overline{E}$ and $\overline{V}$	N and $\overline{A}$	$\overline{F}$	A
				$\overline{R}$	B

k. Use the jumper leads to connect LOAD 1 between the column 1 jacks, in turn, as listed in the chart under *m* below, and set LOAD switch to position 1. Connect LOAD 2 between the column 2 jacks, in turn, as listed in the chart under *m* below, and set LOAD 2 switch to position 1.

l. Connect a jumper lead from the SIGNALS CLOCK PULSE jack to the input jacks, in turn, as indicated in the chart under *m* below.

m. Measure the output logic voltages at the test points indicated in the chart below.

Step No.	Load connection jacks		Input jacks	Test points	Output voltage
	Column 1	Column 2			
1	C and GRD	V and GRD	$\overline{L}$	E	0
			$\overline{L}$	P	−6
			$\overline{N}$	P	0
			$\overline{N}$	E	−6
2	D and GRD	W and GRD	N	E	0
			N	P	−6
			$\overline{A}$	P	0
			$\overline{A}$	E	−6
3	$\overline{D}$ and GRD	$\overline{W}$ and GRD	$\overline{L}$	$\overline{P}$	0
			$\overline{L}$	$\overline{E}$	−6
			$\overline{N}$	$\overline{E}$	0
			$\overline{N}$	$\overline{P}$	−6
4	$\overline{C}$ and GRD	$\overline{V}$ and GRD	N	$\overline{P}$	0
			N	$\overline{E}$	−6
			$\overline{A}$	$\overline{E}$	0
			$\overline{A}$	$\overline{P}$	−6

n. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

o. Remove all jumper leads from the test jacks.

p. Return all TRUE-FALSE switches to the neutral positions.

q. Remove the card assembly from the test jacks.

r. Return all controls and switches to the pretest positions.

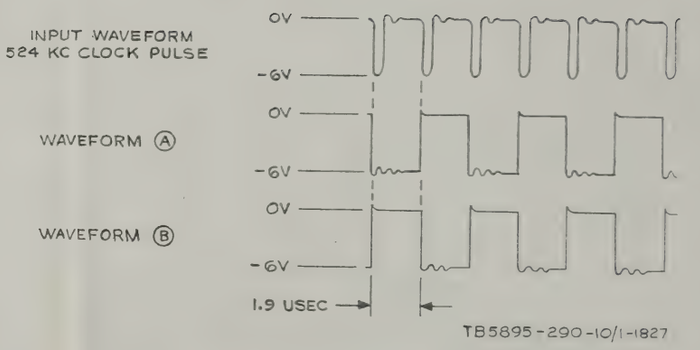


Figure 10. Fast flip-flop card assembly 547514, waveform diagram.

29. Video Coaxial Line Driver Card Assembly 547536

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switch M to TRUE.

b. Set the AC VAR FREQUENCY switch to 1KC.

c. Set the REF PULSE AMPLITUDE switch to +, and adjust the REF PULSE AMPLITUDE control for a 2-volt output.

d. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 100-μsec pulse width.

e. Connect jumper leads from jack F to SIGNALS REF PULSE and from jack A to DC VOLTAGES −50.

f. Connect a load between jacks X and GRD with jumper leads, and set the LOAD selector switch to position 1.

g. Insert card assembly 547536 into test jack.

h. Press the ENERGIZE switch on.

i. Readjust the REF PULSE AMPLITUDE control for a 2-volt output.

j. Readjust the REF PULSE DURATION control for a 100-μsec pulse width.

k. Observe that the waveform at jack X is a 0-volt to +25 volts positive pulse, 100 μsec. in duration. Note that input and output waveforms are in phase.

l. Press the ENERGIZE switch off.

m. Remove all jumper leads from the jacks.

n. Return all TRUE-FALSE switches to the neutral positions.

o. Return all switches and controls to the pretest positions.

30. Analog Sweep Switch Card Assembly 547716

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switches −28 and 28 on.

b. Press SELECT switch 5 on.

c. Set TRUE-FALSE switches K, M, $\overline{K}$, and $\overline{M}$ to TRUE, and $\overline{B}$ to FALSE.

d. Set the AC VAR FREQUENCY switch to 1KC.

e. Press REF PULSE switch on.

f. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

g. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

h. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

i. Insert card assembly 547716 into test jack J1.

j. Press the ENERGIZE switch on.

k. Readjust the REF PULSE AMPLITUDE control for a −6-volt output.

l. Readjust the REF PULSE DURATION control for a 500-μsec pulse width.

m. Measure 0 volt at jacks H, $\overline{H}$, N, $\overline{N}$, P, and $\overline{P}$.

n. Set TRUE-FALSE switch K to the neutral position.

o. Connect jumper leads from jack K to SIGNALS REF PULSE and from jack L to DC VOLTAGES 8.

p. Observe a 1-kc, 6 volt, square wave at jack H.

q. Connect LOAD 1 between jacks $\overline{D}$ and DC VOLTAGES −28 with jumper leads, and set the LOAD 1 selector switch to position 1. Connect LOAD 2 between jacks $\overline{E}$ and GND with jumper leads and set the LOAD 2 selector switch to position 5.

r. Measure −6 volts at jacks P and $\overline{P}$ and 0 volt at jack H.

s. Observe a 1–kc, 8 volt, square wave at jack N.

t. Set TRUE-FALSE switch $\overline{K}$ to neutral.

u. Remove the jumper lead from jack K, and connect to jack $\overline{K}$.

v. Remove the jumper lead from jack L, and connect to jack $\overline{L}$.

w. Measure 0 volt at jack $\overline{H}$.

x. Observe a 1–kc, 8 volt, square wave at jack $\overline{N}$.

y. Remove the jumper leads from jacks $\overline{D}$ and $\overline{E}$.

z. Observe a 1–kc, 6 volt, square wave at jack $\overline{H}$.

aa. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

ab. Remove all jumper leads from the jacks.

ac. Remove the card assembly from the test jack.

ad. Return all TRUE-FALSE switches to the neutral positions.

ae. Return all switches and controls to the pretest positions.

31. Light Control Amplifier Card Assembly 547724

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches M, L, $\overline{A}$, and $\overline{N}$ to TRUE.

b. Press VOLTAGES switch 28 on.

c. Press SELECT switch 5 on.

d. Set the AC VAR FREQUENCY switch to 1KC.

e. Press the REF PULSE switch on.

f. Synchronize the oscilloscope for a negative signal and connect the the SYNC SIGNAL connector.

g. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for −6 volts output.

h. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec output.

i. Connect a jumper lead from jack C to DC VOLTAGES 12.

j. Connect a load between jack E and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 3.

k. Connect a type 327 lamp (FSN 6240–155–7836) between jack N and GRD.

l. Insert card assembly 547724 into test jack J1.

m. Press the ENERGIZE switch on.

n. Readjust the REF PULSE AMPLITUDE control for −6-volt output.

o. Readjust the REF PULSE DURATION control for a 500-μsec pulse width.

p. Set TRUE-FALSE switch L to FALSE.

q. Observe that the 327 lamp goes on.

r. Set TRUE-FALSE switch L to TRUE.

s. Observe that the 327 lamp goes out.

t. Remove the jumper lead from jack E and connect to jack U.

u. Connect the 327 lamp between jack $\overline{D}$ and GRD.

v. Set TRUE-FALSE switch $\overline{A}$ to FALSE.

w. Observe that the 327 lamp goes on.

x. Set TRUE-FALSE switch $\overline{A}$ to TRUE.

y. Observe that the 327 lamp goes out.

z. Remove the jumper lead from jack U and connect to jack $\overline{P}$.

aa. Connect the 327 lamp between jack $\overline{J}$ and GRD.

ab. Set TRUE-FALSE switch $\overline{N}$ to FALSE.

ac. Observe that the 327 lamp goes on.

ad. Set TRUE-FALSE switch $\overline{N}$ to TRUE.

ae. Observe that the 327 lamp goes out.

af. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

ag. Set all TRUE-FALSE switches to the neutral positions.

ah. Return all switches and controls to the pretest positions.

ai. Remove the card assembly from the test jack.

32. Matrix Card Assembly 547864

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, P, R, S, T, U, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 547864 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R $\overline{T}$		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6
II		E $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		E $\overline{E}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		E $\overline{R}$		
	1	t t	$\overline{B}$	0
	2	f t	$\overline{B}$	−6
	3	t f	$\overline{B}$	−6
V		S $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		F $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		F $\overline{F}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VIII		F $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		T $\overline{S}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
X		H $\overline{S}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6
XI		$\overline{H}$ $\overline{P}$		
	1	t t	$\overline{X}$	0
	2	f t	$\overline{X}$	−6
	3	t f	$\overline{X}$	−6
XII		$\overline{P}$ $\overline{U}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		P $\overline{U}$		
	1	t t	L	0
	2	f t	L	−6
	3	t f	L	−6
XIV		K $\overline{U}$		
	1	t t	Y	0
	2	f t	Y	−6
	3	t f	Y	−6
XV		K $\overline{J}$		
	1	t t	$\overline{M}$	0
	2	f t	$\overline{M}$	−6
	3	t f	M	−6
XVI		K $\overline{N}$		
	1	t t	$\overline{A}$	0
	2	f t	$\overline{A}$	−6
	3	t f	$\overline{A}$	−6
XVII		U $\overline{N}$		
	1	t t	M	0
	2	f t	M	−6
	3	t f	M	−6
XVIII		J $\overline{N}$		
	1	t t	Z	0
	2	f t	Z	−6
	3	t f	Z	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

33. Matrix Card Assembly 547865

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, L, R, S, T, U, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 547865 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R $\overline{S}$		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6
II		E $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		E $\overline{F}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		E $\overline{U}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		S $\overline{U}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		F $\overline{U}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		F $\overline{E}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VIII		F $\overline{R}$		
	1	t t	$\overline{B}$	0
	2	f t	$\overline{B}$	−6
	3	t f	$\overline{B}$	−6
IX		T $\overline{R}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
X		H $\overline{R}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6
XI		H $\overline{H}$		
	1	t t	$\overline{X}$	0
	2	f t	$\overline{X}$	−6
	3	t f	$\overline{X}$	−6
XII		H $\overline{T}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		J $\overline{A}$		
	1	t t	$\overline{L}$	0
	2	f t	$\overline{L}$	−6
	3	t f	$\overline{L}$	−6
XIV		J $\overline{N}$		
	1	t t	Z	0
	2	f t	Z	−6
	3	t f	Z	−6
XV		U $\overline{N}$		
	1	t t	K	0
	2	f t	K	−6
	3	t f	K	−6
XVI		L $\overline{N}$		
	1	t t	Y	0
	2	f t	Y	−6
	3	t f	Y	−6
XVII		L $\overline{J}$		
	1	t t	$\overline{M}$	0
	2	f t	$\overline{M}$	−6
	3	t f	$\overline{M}$	−6
XVIII		L $\overline{P}$		
	1	t t	$\overline{K}$	0
	2	f t	$\overline{K}$	−6
	3	t f	$\overline{K}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

34. Switch Card Assembly 547866

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set the CLOCK PULSE FREQUENCY KC selector switch to 50.

b. Set the CLOCK PULSE VAR/−6V switch to −6V.

c. Connect a jumper lead from jack A to SIGNALS CLOCK PULSE.

d. Set switches S1–S9, on card assembly, to OFF.

e. Insert card assembly 547866 into test jack.

f. Connect a load between output jacks and GRD with jumper lead in the sequence given in the chart below. Set the LOAD selector switch to position 4 and measure 0 volt at each output jack indicated.

Step No.	Output jack
1	F
2	H
3	J
4	L
5	T
6	$\overline{H}$
7	$\overline{P}$
8	$\overline{R}$
9	$\overline{S}$

g. Observe −3-volt, 50-kc clock pulses at each output jack listed below. For each step connect a load between output jack and GND with jumper leads and set the LOAD selector switch to position 4. Set switch to ON, observe that the output waveform corresponds to the input at jack A.

Step No.	Switch (on card assembly)	Output jack
1	S1	L
2	S2	$\overline{R}$
3	S3	$\overline{P}$
4	S4	J
5	S5	H
6	S6	$\overline{H}$
7	S7	T
8	S8	$\overline{S}$
9	S9	F

h. AC VAR FREQUENCY switch to 1KC.

i. Press the REF PULSE switch on.

j. Set the REF PULSE DURATION switch to long, and adjust the REF PULSE DURATION control for 500 μsec.

k. Set the REF PULSE AMPLITUDE switch to +.

l. Set the REF PULSE AMPLITUDE control to −6V.

m. Synchronize the oscilloscope to the SYNC SIGNAL jack.

n. Set load switch to position 10.

o. Connect the load between SIGNALS REF PULSE jack and jack A.

p. Connect the oscilloscope to jack A.

q. Observe that the 0 to 85 percent risetime of capacitors C1 through C9 is between 160 and 240 μsec as the switches are set to the TRUE position in the sequence given in the chart below. Also insure that each switch is returned to the neutral position as each step is completed.

Step	Switch	Capacitor checked
1	L	C1
2	$\overline{R}$	C2
3	$\overline{P}$	C3
4	J	C4
5	H	C5
6	$\overline{H}$	C6
7	T	C7
8	$\overline{S}$	C8
9	F	C9

r. Disconnect the load and oscilloscope from jack A and connect them to jack Y. Observe that the 0 to 85 percent risetime of capacitors C10 through C20 is between 160 and 240 μsec as the switches are set to the true position in the sequence given in the chart below. Also insure that each switch is returned to the neutral position as each step is completed.

Step	Switch	Capacitor checked
1	R	C10
2	$\overline{M}$	C11
3	K	C12
4	$\overline{N}$	C13
5	S	C14
6	$\overline{L}$	C15
7	M	C16
8	N	C17
9	$\overline{K}$	C18
10	P	C19
11	J	C20

s. Remove all jumper leads from jacks.

t. Remove the card assembly from the test jack.

u. Return all switches and controls to the pretest positions.

35. Skimmer Matrix and Test Card Assembly 547867

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Press VOLTAGES switches 1.5, −7.5, 28, 50, and −50 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches M to TRUE, and C, E, F, H, K, P, R, S, T, U, Y, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 50.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

g. Insert card assembly 547867 into test jack.

h. Set the VIDEO COUNT TEST switch, on the card assembly, to NORM and the SKIM COUNT TEST switch, on the card assembly, to TEST.

i. Press the ENERGIZE switch on.

j. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false) Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test. All test points designated as TP are on the card assembly.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		C $\overline{A}$ $\overline{K}$		
	1	t t t	$\overline{V}$, TP2	0
	2	f t t	$\overline{V}$, TP2	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
II		C $\overline{A}$ $\overline{P}$		
	1	t t t	$\overline{B}$, TP3	0
	2	f t t	$\overline{B}$, TP3	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6
III		F $\overline{E}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		F $\overline{R}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		R $\overline{R}$		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6
VI		H $\overline{R}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		Y U $\overline{H}$ $\overline{N}$		
	1	t t t t	TP1	0
	2	f t t f	TP1	−6
	3	t f t f	TP1	−6
	4	t t f f	TP1	−6
	5	t t t f	TP1	0
	6	f f f t	TP1	0
VIII		S T $\overline{N}$ $\overline{T}$ $\overline{U}$[a]		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	5	t t f t t	$\overline{V}$	−6
	6	t t t f t	$\overline{V}$	−6
	7	t t t t f	$\overline{V}$	−6
IX		E K $\overline{T}$[a]		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	0
	3	t f t	$\overline{B}$	0
	4	t t f	$\overline{B}$	−6
	5	f f t	$\overline{B}$	−6
X		P $\overline{P}$[b]		
	1	t t	D	Clock pulses
	2	f t	D	−6
	3	t f	D	0
XI		F $\overline{P}$[b]		
	1	t t	W	Clock pulses
	2	f t	W	−6
	3	t f	W	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XII		$\overline{F}$ $\overline{P}$[b]		
	1	t t	$\overline{X}$	Clock pulses
	2	f t	$\overline{X}$	−6
	3	t f	$\overline{X}$	0
XIII		$\overline{P}$ $\overline{S}$[b]		
	1	t t	$\overline{D}$	Clock pulses
	2	f t	$\overline{D}$	0
	3	t f	$\overline{D}$	−6
XIV		P R $\overline{E}$ $\overline{P}$[c]		
	1	t t t t	$\overline{D}$	−6
			TP6	0.6
	2	f t t t	$\overline{D}$	−6
			TP6	0.6
	3	t f t t	$\overline{D}$	−6
			TP6	0.6
	4	t t f t	$\overline{D}$	−6
			TP6	0.6
	5	t t t f	$\overline{D}$	0
			TP6	−0.5
	6	f f f t	$\overline{D}$	0
			TP6	−0.5

[a] Set SKIM COUNT TEST switch, on card assembly, to NORM.

[b] Set TRUE-FALSE switch R to TRUE. Connect a jumper lead between jack J and SIGNALS CLOCK PULSE. Observe clock pulses at TP4.

[c] Remove jumper lead from jack J and set VIDEO COUNT TEST switch to TEST. Set TRUE-FALSE switches $\overline{A}$ to FALSE and $\overline{S}$ to TRUE.

k. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

l. Remove all jumper leads from the jacks.

m. Return all TRUE-FALSE switches to the neutral position.

n. Set the AC VAR FREQUENCY switch to 1 KC.

o. Press the REF PULSE switch on.

p. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

q. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a 6-volt output.

r. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec width.

s. Set TRUE-FALSE switch $\overline{P}$ to TRUE.

t. Connect a load between jack $\overline{L}$ and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 9.

u. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack $\overline{L}$ is 40 to 50 μsec.

v. Remove the jumper lead from jack $\overline{L}$ and connect to jack L.

w. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack L is 40 to 50 μsec.

x. Remove the jumper lead from jack L and connect to jack $\overline{N}$.

y. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack N is 40 to 50 μsec.

z. Remove all jumper leads from the jacks.

aa. Remove the card assembly from the test jack.

ab. Return all switches and controls to the pretest positions.

36. Up-down Counter Stop and Test Card Assembly 547869

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switches −7.5 and 28 on.

b. Press SELECT switches 7 and 5 on.

c. Set TRUE-FALSE switches M to TRUE and $\overline{B}$ to FALSE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 50.

e. Set the CLOCK PULSE VAR/−6V switch to to −6V.

f. Connect a jumper lead from jack $\overline{P}$ to SIGNALS CLOCK PULSE.

g. Insert card assembly 547869 into test jacks.

h. Set the COUNT DOWN TEST-NORM switch, S1 on the card assembly, to NORM.

i. Press the ENERGIZE switch on.

j. Set TRUE-FALSE switch $\overline{K}$ to TRUE.

k. Observe −6-volt clock pulses at jack $\overline{L}$ and TP1 and TP2 (on card assembly).

l. Set TRUE-FALSE switch $\overline{K}$ to FALSE.

m. Observe that the clock pulses disappear from jack $\overline{L}$ and TP1 and TP2.

n. Remove the jumper lead from jack-$\overline{P}$ and connect to jack S.

o. Set the COUNT UP TEST-NORM switch, S2 on the card assembly, to NORM.

p. Set TRUE-FALSE switch $\overline{F}$ to TRUE.

q. Observe clock pulses at jack N and TP3 and TP4 (on card assembly).

r. Set TRUE-FALSE switch $\overline{F}$ to FALSE.

s. Observe that the clock pulses at jack N, TP3 and TP4 disappear.

t. Set TRUE-FALSE switch $\overline{A}$ to FALSE.

u. Set the COUNT DOWN TEST-NORM and the COUNT UP TEST-NORM switches, on card assembly, to TEST.

v. Measure −6 volts at jacks N and $\overline{L}$.

w. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

x. Remove all jumper leads from the jacks.

y. Return all TRUE-FALSE switches to the neutral positions.

z. Remove the card assembly from the test jack.

aa. Return all switches and controls to the pretest positions.

37. Range Gate and Video Skimmer Card Assembly 547870

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Press VOLTAGES switches 1.5, −7.5, −28, and −50, and 50 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches M to TRUE and $\overline{B}$ to FALSE.

d. Set CLOCK PULSE FREQUENCY KC selector switch to 50.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

f. Connect jumper leads from jack $\overline{X}$ to DC VOLTAGES 1.5.

g. Connect LOAD 1 between jacks $\overline{L}$ and GRD with jumper leads, and set LOAD 1 selector switch to position 4. Connect LOAD 2 between jacks $\overline{V}$ and GRD with jumper leads, and set the LOAD 2 selector switch to position 4.

h. Connect a jumper lead from jack $\overline{S}$ to SIGNALS CLOCK PULSE.

i. Insert card assembly 547810 into test jack J1.

j. Set the MAN-AUTO switch S1, on card assembly, to AUTO.

k. Press the ENERGIZE switch on.

l. Observe −6 volt, 50-kc pulses at jacks $\overline{F}$ and $\overline{W}$.

m. Observe that the −6 volt, 50-kc pulses at jack $\overline{D}$ are delayed 3-μsec from the input pulses at jack $\overline{S}$.

n. Set TRUE-FALSE switch $\overline{P}$ to TRUE, and observe −2 volt, 50-kc pulses at jack $\overline{L}$. Set TRUE-FALSE switch $\overline{P}$ to FALSE and observe that the pulses at jack $\overline{L}$ disappear.

o. Set TRUE-FALSE switch E to TRUE and observe −6 volt, 50-kc pulses at jack V. Set TRUE-FALSE switch E to FALSE and measure −6 volts at jack V.

p. Set TRUE-FALSE switch N to TRUE and measure 0 volt at jack H and −6 volts at jack F.

q. Set TRUE-FALSE switch N to FALSE and measure 0 volt at jack F and −6 volts at jack H.

r. Remove the jumper lead from jack $\overline{S}$ and connect to jack J.

s. Connect a 2,200 ohm resistor between jack J and DC VOLTAGES 12.

t. Set TRUE-FALSE switches E, $\overline{K}$, $\overline{P}$, and $\overline{R}$ to FALSE.

u. Observe that the −2 volt, 50-kc pulses at jack $\overline{V}$ are delayed .95 μsec from the input pulses at jack J.

v. Set TRUE-FALSE switches $\overline{P}$ and $\overline{R}$, in turn, to TRUE and then to FALSE. Observe that the pulses at jack $\overline{V}$ disappear when each switch is in the TRUE position.

w. Observe −6 volt, 50-kc pulses at jack C.

x. Set TRUE-FALSE switches E and $\overline{K}$, in turn, to TRUE and then to FALSE. Observe that the pulses at jack C disappear when each switch is in the TRUE position.

y. Set the AC VAR FREQUENCY switch to VAR and adjust the AC VAR FREQUENCY control for a 5-kc output.

z. Set the REF PULSE AMPLITUDE switch to +, and adjust the REF PULSE AMPLITUDE control for a 2.5-volt output.

aa. Set the REF PULSE DURATION switch to SHORT, and adjust the REF PULSE DURATION control for a 2-μsec pulse width.

ab. Connect a jumper lead between jack $\overline{T}$ and SIGNALS REF PULSE.

ac. Observe 2-μsec, 5-kc, −6-volt pulses at jack B referenced to 28 volts, (28 to 22 volts).

ad. Set AUTO-MAN switch S1, on card assembly, to MAN, and observe that R7, on card assembly, adjusts the amplitude of the pulses, at jack B, from 0 to 10 volts.

ae. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

af. Remove all jumper leads from the jacks.

ag. Return all TRUE-FALSE switches to the neutral positions.

ah. Remove the card assembly from the test jack.

ai. Return all switches and controls to the pretest positions.

38. Digilog and Blocking Oscillator Card Assembly 547872

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switches 1.5, −7.5, −28, 28, −50, 50, and 150 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches M to TRUE and $\overline{B}$ to FALSE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 50.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

f. Connect a jumper lead between jacks C and SIGNALS CLOCK PULSE.

g. Connect a load between jack C and DC VOLTAGES 12 with jumper leads and set the LOAD selector switch to position 6.

h. Insert card assembly 547872 into test jack J1.

i. Press the ENERGIZE switch on.

j. Observe −6V, 50–kc pulses at jack $\overline{L}$.

k. Remove the jumper lead from jack C and connect to jack $\overline{K}$.

l. Set TRUE-FALSE switches E and $\overline{P}$ to TRUE and observe −6V, 50–kc pulses at jack $\overline{V}$ and $\overline{U}$.

m. Set TRUE-FALSE switches E to FALSE and $\overline{P}$ to TRUE, and then E to TRUE and $\overline{P}$ to FALSE. Observe that the −6V, 50–kc pulses remain at jack $\overline{V}$ under each of the conditions.

n. Set TRUE-FALSE switches E and $\overline{P}$ to FALSE and observe that the pulses at jack $\overline{V}$ disappear.

o. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

p. Remove all jumper leads from the jacks.

q. Return all TRUE-FALSE switches to the neutral positions.

r. Measure the resistance between jacks listed below.

Jacks	Resistance (ohms)
V M	680
W M	680
K $\overline{T}$	7900
$\overline{T}$ J	7900
J $\overline{S}$	7900
$\overline{S}$ H	7900
H $\overline{R}$	7900
$\overline{R}$ $\overline{F}$	7900
M F	5600

s. Remove the card assembly from the test jack.

t. Return all switches and controls to the pretest position.

39. Matrix Card Assembly 547874

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, T, U, W, X, Y, $\overline{D}$, $\overline{L}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Connect a load between jacks $\overline{B}$ and DC VOLTAGES 50 with jumper leads, and set LOAD switch to position 8.

d. Press SELECT switch 1 on.

e. Insert matrix assembly 547874 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{S}$ $\overline{T}$ $\overline{U}$ $\overline{W}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
II		$\overline{D}$	$\overline{C}$	0
	1	t		
	2	f	$\overline{C}$	−6
III		E F H J N P		
	1	t t t t t t	D	0
	2	f t t t t t	D	−6
	3	t f t t t t	D	−6
	4	t t f t t t	D	−6
	5	t t t f t t	D	−6
	6	t t t t f t	D	−6
	7	t t t t t f	D	−6
IV		H K N P W		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		L W		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		E H J S		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		T		
	1	t	V	0
	2	f	V	−6
VIII		U		
	1	t	V	0
	2	f	V	−6
IX		$\overline{L}$		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
X		T		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
XI		R Y		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XII		P T Y		
	1	t t t	B	0
	2	f t t	B	−6
	3	t f t	B	−6
	4	t t f	B	−6
XIII		U X Y		
	1	t t t	B	0
	2	f t t	B	−6
	3	t f t	B	−6
	4	t t f	B	−6
XIV		J N P T U W $\overline{L}$ $\overline{W}$		
	1	t t t t t t t t	$\overline{B}$	0
	2	f t t t t t t t	$\overline{B}$	−6
	3	t f t t t t t t	$\overline{B}$	−6
	4	t t f t t t t t	$\overline{B}$	−6
	5	t t t f t t t t	$\overline{B}$	−6
	6	t t t t f t t t	$\overline{B}$	−6
	7	t t t t t f t t	$\overline{B}$	−6
	8	t t t t t t f t	$\overline{B}$	−6
	9	t t t t t t t f	$\overline{B}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

40. RHI Video Intensity/Blanking Pedestal Generator Card Assembly 547875

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Press VOLTAGES switches −7.5, −28, 28, and 50 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches M to TRUE and $\overline{B}$ to FALSE.

d. Set the AC VAR FREQUENCY switch to 1KC.

e. Press the REF PULSE switch on.

f. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNALS connector.

g. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

h. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

i. Connect jumper leads from jacks A, E, and R to SIGNALS REF PULSE.

j. Insert card assembly 547875 into test jack J1.

k. Press the ENERGIZE switch on.

l. Readjust the REF PULSE AMPLITUDE control for a −6-volt output.

m. Readjust the REF PULSE DURATION control for a 500-μsec pulse width.

n. Observe a −6-volt, 1-kc waveform at jacks $\overline{F}$ and $\overline{J}$ 180° out of phase with the input waveform.

o. Observe that the waveform at jack C corresponds with the output waveform shown on figure 11.

p. Observe that the upper portion of the waveform at jack C varies from 0 to 1.2 volts by adjusting VIDEO PED AMPL CONTROL 1 on the card assembly.

q. Observe that the waveform at jack $\overline{D}$ corresponds with the output waveform shown on figure 11.

r. Observe that the upper portion of the waveform at jack $\overline{D}$ varies from 0 to 1.2 volts by adjusting VIDEO PED AMPL CONTROL 2 on the card assembly.

s. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

t. Remove all jumper leads from the jacks.

u. Remove the card assembly from the test jack.

v. Return all switches and controls to the pretest positions.

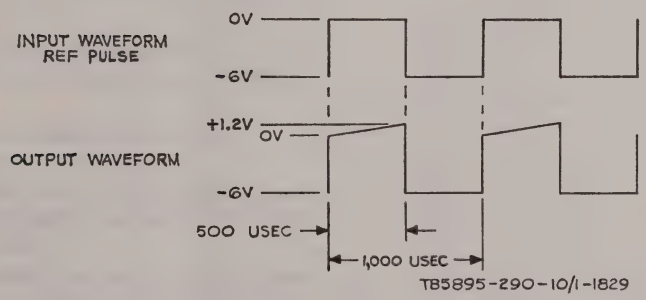


Figure 11. RHI video intensity/blanking pedestal generator card assembly 547875, waveform diagram.

41. Marker and Azimuth Cursor Gate Card Assembly 547876

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Press VOLTAGES switches −7.5, 1.5, −28, and 28 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switches A to TRUE and $\overline{B}$ to FALSE.

d. Set the AC VAR FREQUENCY switch to VAR, and adjust the AC VAR FREQUENCY control for a 5-kc output.

e. Adjust the AC VAR AMPLITUDE control for 2-volt output.

f. Connect a jumper lead between jack C and SIGNALS AC VARIABLE, and between jack $\overline{W}$ and SIGNALS AC VARIABLE.

g. Insert card assembly 547876 into test jack J1.

h. Press the ENERGIZE switch on.

i. Press the + DC VAR 1 switch on and adjust DC VAR 1 control for a 6-volt output.

j. Connect a jumper lead between jack H and DC VAR 1. Readjust the + DC VAR 1 control for a 6-volt output.

k. Set TRUE-FALSE switches K to TRUE and B and E to FALSE.

l. Observe a 1-volt, 5-kc sine wave at jacks R and J.

m. Set TRUE-FALSE switch E to TRUE.

n. Observe a 1.5-volt, 5-kc sine wave at jacks R and J.

o. Measure −6 volts at jacks D and $\overline{V}$.

p. Set TRUE-FALSE switches B to TRUE and K to FALSE.

q. Measure 0 volt at jacks D, R, J, and $\overline{V}$.

r. Press ENERGIZE switch to off.

s. Remove jumper leads between jack C and SIGNALS AC VARIABLE and jack $\overline{W}$ and SIGNALS AC VARIABLE.

t. Connect a jumper lead between jack D and SIGNALS DSW and between jack $\overline{V}$ and SIGNALS DSW.

u. Set TRUE-FALSE switches B and E to FALSE.

v. Set CLOCK PULSE FREQUENCY KC to 170.

w. Set the CLOCK PULSE AMPLITUDE switch to −6V.

x. Synchronize oscilloscope for a negative signal to the SYNC SIGNAL connector.

y. Press ENERGIZE switch on.

z. Observe that the waveform at jacks R and J is a −6 ±.5 volt, 170 kc square wave.

aa. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

ab. Remove all jumper leads from the jacks.

ac. Remove the card assembly from the test jack.

ad. Return all switches and controls to the pretest position.

42. Matrix Card Assembly 547878

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, J, P, W, X, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{N}$, $\overline{P}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 547878 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

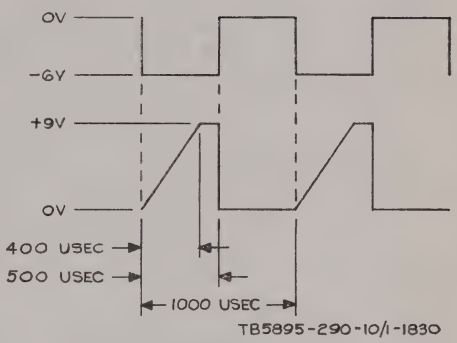
Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		W $\overline{N}$ $\overline{S}$		
	1	t t t	$\overline{R}$	0
	2	f t t	$\overline{R}$	−6
	3	t f t	$\overline{R}$	−6
	4	t t f	$\overline{R}$	−6
II		P W X $\overline{N}$		
	1	t t t t	$\overline{R}$	0
	2	f t t t	$\overline{R}$	−6
	3	t f t t	$\overline{R}$	−6
	4	t t f t	$\overline{R}$	−6
	5	t t t f	$\overline{R}$	−6
III		J $\overline{H}$		
	1	t t	K	0
	2	f t	K	−6
	3	t f	K	−6
IV		X $\overline{P}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		$\overline{A}$ D $\overline{E}$		
	1	t t t	Y	0
	2	f t t	Y	−6
	3	t f t	Y	−6
	4	t t f	Y	−6
VI		$\overline{B}$ D $\overline{E}$		
	1	t t t	H	0
	2	f t t	H	−6
	3	t f t	H	−6
	4	t t f	H	−6
VII		$\overline{E}$ $\overline{F}$ $\overline{H}$		
	1	t t t	$\overline{T}$	0
	2	f t t	$\overline{T}$	−6
	3	t f t	$\overline{T}$	−6
	4	t t f	$\overline{T}$	−6
VIII		F $\overline{F}$		
	1	t t	C	0
	2	f t	C	−6
	4	t f	C	−6
IX		E		
	1	t	D	0
	2	f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.



zimuth curser generator card assembly 547879, waveform diagram.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		$\overline{A}$ $\overline{D}$ $\overline{E}$		
	1	t t t	Y	0
	2	f t t	Y	−6
	3	t f t	Y	−6
	4	t t f	Y	−6
VI		$\overline{B}$ $\overline{D}$ $\overline{E}$		
	1	t t t	H	0
	2	f t t	H	−6
	3	t f t	H	−6
	4	t t f	H	−6
VII		$\overline{E}$ $\overline{F}$ $\overline{H}$		
	1	t t t	$\overline{T}$	0
	2	f t t	$\overline{T}$	−6
	3	t f t	$\overline{T}$	−6
	4	t t f	$\overline{T}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		F $\overline{F}$		
	1	t t	C	0
	2	f t	C	−6
	4	t f	C	−6
IX		E		
	1	t	D	0
	2	f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

43. Azimuth Cursor Generator Card Assembly 547879

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches M and $\overline{R}$ to TRUE, and $\overline{B}$, F, H, P, R, and S to FALSE.

b. Press VOLTAGES switches −7.5, −28, 28, −50, and 50 on.

c. Press SELECT switch 1 on.

d. Connect jumper leads from jack W to DC VOLTAGES −7.5, jack $\overline{K}$ to DC VOLTAGES 28, and from jack Z to SIGNALS REF PULSE.

e. Connect a load between jack $\overline{C}$ and GRD with jumper leads, and set the LOAD selector switch to position 4.

f. Set the AC VAR FREQUENCY switch to 1KC.

g. Press the REF PULSE switch on.

h. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

i. Set the REF PULSE AMPLITUDE switch to −, and adjust REF PULSE AMPLITUDE control for −6 volts output.

j. Set the REF PULSE DURATION switch to LONG, and adjust REF PULSE DURATION control for a 500-μsec pulse width.

k. Insert card assembly 547879 into test jack J1.

l. Press the ENERGIZE switch on.

m. Readjust the REF PULSE AMPLITUDE control for a 6-volt output.

n. Readjust the REF PULSE DURATION control for a 500-μsec pulse width.

o. Observe that the waveform at TP1 corresponds to the input waveform shown on figure 12.

p. Observe that the waveform at jack $\overline{C}$ and TP4 corresponds to the output waveform shown on figure 12. If the amplitude of the output waveform is not +9V, adjust it to +9V by means of AZIMUTH CURSOR AMPLITUDE control R27.

q. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F		
	1	t	TP2	−3
	2	f	PT2	−7
II		H		
	1	t	TP2	−3
	2	f	TP2	−7
III		R		
	1	t	TP2	−3
	2	f	TP2	−7
IV		F		
	1	t	T	−6
	2	f	T	0
V		H		
	1	t	T	−6
	2	f	T	0
VI		R		
	1	t	T	−6
	2	f	T	0
VII		P		
	1	t	TP3	−3
	2	f	TP3	−7
VIII		R		
	1	t	TP3	−3
	2	f	TP3	−7
IX		S		
	1	t	TP3	−3
	2	f	TP3	−7
X		P		
	1	t	U	−6
	2	f	U	0
XI		R		
	1	t	U	−6
	2	f	U	0
XII		S		
	1	t	U	−6
	2	f	U	0

r. Press ENERGIZE, VOLTAGES, and SELECT switches off.

s. Return all TRUE-FALSE switches to the neutral positions.

t. Remove all jumper leads from the jacks.

u. Remove the card assembly from the test jack.

v. Return all switches and controls to pretest positions.

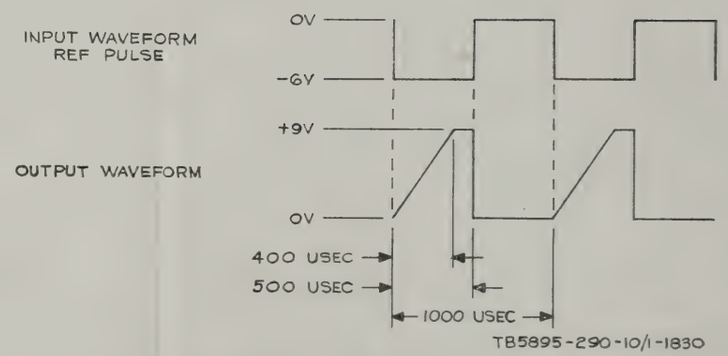


Figure 12. Azimuth curser generator card assembly 547879, waveform diagram.

44. Composite Video Gate Card Assembly 547880

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switches 1.5, −7.5, −28, 28, −50, and 50 on.

b. Press SELECT switch 1 and REF PULSE switch on.

c. Set TRUE-FALSE switches D and M to TRUE and $\overline{B}$ to FALSE.

d. Set the REF PULSE AMPLITUDE switch to +, and adjust the REF PULSE AMPLITUDE control for an 8-volt output.

e. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

f. Connect a jumper lead from jack C to SIGNALS REF PULSE.

g. Set AC VAR FREQUENCY switch to 1 KC position.

h. Insert card assembly 547880 into test jack J1, and press the ENERGIZE switch on.

i. Readjust the REF PULSE AMPLITUDE control for an 8-volt output.

j. Readjust the REF PULSE DURATION control for 500-μsec pulse width.

k. Set TRUE-FALSE switches K and $\overline{A}$ to TRUE and measure 0 volt at jack F.

l. Set TRUE-FALSE switch $\overline{A}$ to FALSE.

m. Measure 0 volt at jack F.

n. Set TRUE-FALSE switches K and $\overline{A}$ to FALSE and observe a 7 volt, 1–kc square wave at jack F.

o. Set TRUE-FALSE switch $\overline{A}$ to TRUE and measure 0 volt at jack F.

p. Measure 6 volts at jack H and −7.5 volts at jack $\overline{E}$.

q. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{A}$		
	1	t	N	1.5
	2	f	N	−3
II		E $\overline{A}$ $\overline{U}$		
	1	t t t	$\overline{R}$	−3
	2	f f f	$\overline{R}$	−3
	3	f f t	$\overline{R}$	2.5
	4	t f f	$\overline{R}$	2.5
	5	t f t	$\overline{R}$	2.5
	6	f t f	$\overline{R}$	−3
	7	f t t	$\overline{R}$	−3
	8	t t f	$\overline{R}$	−3
III		J $\overline{P}$		
	1	t t	$\overline{N}$	0
	2	f t	$\overline{N}$	−6
	3	t f	$\overline{N}$	−6
IV		$\overline{K}$		
	1	t	$\overline{L}$	0
	2	f	$\overline{L}$	−6
V		R S T $\overline{F}$		
	1	f f f f	$\overline{T}$	−6
	2	f f f t	$\overline{T}$	0
	3	f f t f	$\overline{T}$	0
	4	f t f f	$\overline{T}$	0
	5	t f f f	$\overline{T}$	0

r. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

s. Remove all jumper leads from the jacks.

t. Measure 47 ohms between jacks M and V.

u. Remove the card assembly from the test jack.

v. Return all TRUE-FALSE switches to the neutral positions.

w. Return all switches and controls to the pretest positions

45. Process ATWS Video and Height Blanking Pedestal Generator Card Assembly 547882

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches M to TRUE and C, D, H, K, L, $\overline{B}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches 28, −28, and −7.5 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jack B and GRD with jumper leads, and set the LOAD selector switch

to position 1. Connect LOAD 2 between jack T and GRD with jumper leads, and set the LOAD 2 switch to position 1.

e. Insert card assembly 547882 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		C		
	1	t	TP1, B	0
	2	f	TP1, B	−6
II		D		
	1	t	TP1, B	0
	2	f	TP1, B	−6
III		H		
	1	t	TP2	0
	2	f	TP2	−6
IV		K		
	1	t	TP2	0
			TP3	−6
	2	f	TP2	−6
			TP3	0
V		L[a]		
	1	t	TP3	0
	2	f	TP3	−6
VI		$\overline{S}$[b]		
	1	t	TP4, T	0
	2	f	TP4, T	−6

[a] Set TRUE-FALSE switch K to TRUE.
[b] Set TRUE-FALSE switch H to TRUE.

h. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to the neutral positions.

k. Remove card assembly from test jacks.

46. Direct Current Power Filter Card Assembly 547885

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switch M to TRUE.

b. Press the REF PULSE switch on, and set AC VAR FREQUENCY switch to 1 KC.

c. Syncronize the oscilloscope for a negative signal and connect to the SIGNAL SYNC connector.

d. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a 10-volt output.

e. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

f. Insert card assembly 547885 into test jack J1.

g. Readjust the REF PULSE AMPLITUDE control for a 10-volt output.

h. Readjust the REF PULSE DURATION control for a 500-μsec output.

i. Connect a jumper lead from jacks SIGNALS REF PULSE to each input jack, in turn, as indicated in the chart below. Observe that the 0 to 85 percent negative-going rise time of the waveform at each output jack is as indicated.

Input jack	Output jack	Rise time (microseconds)
B	A	105 to 175
N	P	50 to 80
V	X	105 to 175
W	Y	105 to 175
$\overline{A}$	Z	105 to 175
$\overline{D}$	$\overline{B}$	105 to 175
$\overline{L}$	$\overline{M}$	105 to 175
$\overline{V}$	$\overline{N}$	50 to 80
$\overline{X}$	$\overline{Y}$	105 to 175

j. Remove all jumper leads from the jacks.

k. Return all TRUE-FALSE switches to the neutral positions.

l. Remove the card assembly from the test jack.

m. Return all switches and controls to the pretest positions.

47. Special Matrix Card Assembly 547901

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Press VOLTAGES switches 1.5, −7.5, and 50 on.

b. Press SELECT switch 1 on.

c. Set TRUE-FALSE switch M to TRUE.

d. Set the CLOCK PULSE FREQUENCY KC selector switch to 50.

e. Set the CLOCK-PULSE VAR/−6V switch to −6V.

f. Connect a jumper lead between jack $\overline{U}$ and SIGNALS CLOCK PULSE.

g. Insert card assembly 547901 into test jack J1.

h. Press the ENERGIZE switch on.

i. Observe that the −6-volt, 50-kc pulses at jack B are delayed 3 microseconds from the input pulses at jack $\overline{U}$.

j. Connect jumper leads from jacks $\overline{U}$ and $\overline{F}$ to SIGNALS CLOCK PULSE.

k. Set TRUE-FALSE switch $\overline{E}$ to TRUE.

l. Observe −6-volt, 50-kc pulses at jacks $\overline{M}$ and $\overline{X}$.

m. Set TRUE-FALSE switch $\overline{E}$ to FALSE and observe that the pulses at jacks $\overline{M}$ and $\overline{X}$ disappear.

n. Remove all jumper leads from the jacks.

o. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R $\overline{T}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		E $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		E $\overline{H}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		E $\overline{S}$		
	1	t f	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		S $\overline{S}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		F $\overline{S}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		F $\overline{J}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VIII		F $\overline{U}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

p. Set the AC VAR FREQUENCY switch to 1 KC.

q. Press the REF PULSE switch on.

r. Synchronize the oscilloscope for a negative signal to the SYNC SIGNAL connector.

s. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a 6-volt output.

t. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec width.

u. Set TRUE-FALSE switch Y to TRUE.

v. Connect a load between jack N and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 8.

w. Observe that the 0 to 83 percent rise time of the negative-going waveform at jack $\overline{N}$ is 15 to 25 μsec.

x. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

y. Return all TRUE-FALSE switches to the neutral positions.

z. Remove the card assembly from the test jack.

aa. Return all switches and controls to the pretest positions.

48. RHI Intensity Pedestal Switch Card Assembly 547947

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches M to TRUE, and W, $\overline{B}$, $\overline{H}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert card assembly 547947 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		W		
	1	t	TP1	0
	2	f	TP1	−6
II		$\overline{H}$		
	1	t	TP1	0
	2	f	TP1	−6
III		$\overline{T}$		
	1	t	TP1	0
	2	f	TP1	−6
IV		W		
	1	t	TP2,N	−6
	2	f	TP2,N	0
V		$\overline{H}$		
	1	t	TP2,N	−6
	2	f	TP2,N	0
VI		$\overline{T}$		
	1	t	TP2,N	−6
	2	f	TP2,N	0

g. Press the ENERGIZE switch off.

h. Remove all jumper leads from the jacks.

i. Remove the card assembly from the test jack.

j. Return all TRUE-FALSE switches to the neutral positions.

49. Matrix Card Assembly 547948

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, J, K, L, M, N, P, S, T, X, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 547948 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F N		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		K		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		S		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IV		$\overline{F}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
V		$\overline{T}$ $\overline{U}$ $\overline{V}$		
	1	t t t	B	0
	2	f t t	B	−6
	3	t f t	B	−6
	4	t t f	B	−6
VI		$\overline{B}$ $\overline{E}$		
	1	t t	Y	0
	2	f t	Y	−6
	3	t f	Y	−6
VII		K		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		$\overline{A}$		
	1	t	H	0
	2	f	H	−6
IX		P		
	1	t	E	0
	2	f	E	−6
X		$\overline{K}$		
	1	t	U	0
	2	f	U	−6
XI		$\overline{H}$		
	1	t	W	0
	2	f	W	−6
XII		L $\overline{R}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XIII		J		
	1	t	V	0
	2	f	V	−6
XIV		S		
	1	t	V	0
	2	f	V	−6
XV		$\overline{F}$		
	1	t	V	0
	2	f	V	−6
XVI		P		
	1	t	C	0
	2	f	C	−6
XVII		J		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XVIII		J		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
XIX		$\overline{S}$		
	1	t	R	0
	2	f	R	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between $\overline{Y}$ and M, $\overline{Y}$ and T, $\overline{Y}$ and X, $\overline{Y}$ and $\overline{L}$, $\overline{Y}$ and $\overline{M}$, $\overline{Y}$ and $\overline{R}$, $\overline{Y}$ and $\overline{S}$, and $\overline{Y}$ and $\overline{X}$.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

50. Marker Intensity Pedestal Generator Card Assembly 547949

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches M to TRUE and $\overline{B}$ to FALSE.

b. Press VOLTAGES switches −7.5 and 1.5 on, and press SELECT switches 5 and 7 on.

c. Connect a jumper lead between jack $\overline{Y}$ and 28 DC VOLTAGES, and jack A and −28 DC VOLTAGES.

d. Synchronize the oscilloscope for a negative signal and connector to the SYNC WORD connector.

e. Set the CLOCK PULSE VAR/−6V switch to −6V.

f. Set the CLOCK PULSE FREQUENCY KC selector switch to 170.

g. Press RANDOM WORD GENERATOR switches 1, 2, and 3 to true.

h. Press the SPECIAL WORD ON switch on.

i. Connect jumper leads from jack $\overline{A}$ to SIGNALS CLOCK PULSE, and from jack $\overline{S}$ to SIGNALS WORD.

j. Insert card assembly 547949 into test jack J1.

k. Press the ENERGIZE switch on.

l. Observe that the waveform at jack $\overline{W}$ is three −6-volt pulses delayed approximately 1-μsec in reference to the clock pulse, see figure 13 waveform Ⓐ.

m. Observe that the waveform at jack $\overline{C}$ is three −6-volt pulses delayed approximately 5-μsec in reference to the clock pulse, see figure 13 waveform Ⓑ.

n. Remove jumper lead from $\overline{S}$ and set TRUE-FALSE switch $\overline{S}$ to FALSE.

o. Measure 0 volt at jacks $\overline{C}$ and $\overline{W}$.

p. Set TRUE-FALSE switch $\overline{E}$ to TRUE.

q. Measure −6 volts at jack P.

r. Set TRUE-FALSE switch $\overline{E}$ to FALSE.

s. Measure 0 volt at jack P.

t. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

u. Remove all jumper leads from the jacks.

v. Return all TRUE-FALSE switches to the neutral positions.

w. Remove the card assembly from the test jack.

x. Return all switches and controls to the pretest positions.

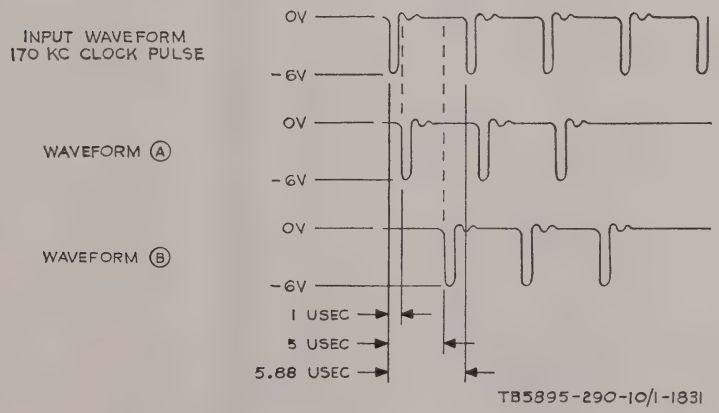


Figure 13. Marker intensity pedestal generator card assembly 547949, waveform diagram.

51. Matrix Card Assembly 547950

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, J, K, L, M, N, S, T, U, V, Z, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 547950 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{N}$ $\overline{P}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
II		$\overline{K}$ $\overline{N}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
III		F Z		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IV		$\overline{M}$ $\overline{R}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
V		F K		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VI		J $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		S		
	1	t	W	0
	2	f	W	−6
VIII		$\overline{F}$		
	1	t	W	0
	2	f	W	−6
IX		L M N T $\overline{H}$		
	1	t t t t t	J	0
	2	f t t t t	J	−6
	3	t f t t t	J	−6
	4	t t f t t	J	−6
	5	t t t f t	J	−6
	6	t t t t f	J	−6
X		E M T U $\overline{H}$		
	1	t t t t t	J	0
	2	f t t t t	J	−6
	3	t f t t t	J	−6
	4	t t f t t	J	−6
	5	t t t f t	J	−6
	6	t t t t f	J	−6
XI		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XII		$\overline{L}$ $\overline{P}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XIII		$\overline{S}$		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
XIV		L M N T $\overline{H}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XV		E M T U $\overline{H}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVI		$\overline{E}$ V		
	1	t t	$\overline{A}$	0
	2	f t	$\overline{A}$	−6
	3	t f	$\overline{A}$	−6
XVII		$\overline{K}$ $\overline{N}$		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6
XVIII		$\overline{T}$		
	1	t	C	0
	2	f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and H, $\overline{Y}$ and P, $\overline{Y}$ and R, and $\overline{Y}$ and X.

j. Remove the matrix assembly from the test jack.

52. IFF/Surveillance Video Amplifier Card Assembly 547955

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switch 28 on.

b. Press SELECT switch 5 on.

c. Set TRUE-FALSE switches M, V, X, and Y to TRUE and $\overline{B}$ to FALSE.

d. Set the AC VAR FREQUENCY switch to VAR and adjust the AC VAR FREQUENCY control for a 5-kc output.

e. Set the REF PULSE AMPLITUDE switch to + and adjust the REF PULSE AMPLITUDE control for a 2-volt output.

f. Set REF PULSE DURATION switch to SHORT, and adjust the REF PULSE DURATION control for 4-μsec pulse width.

g. Connect a jumper lead between jack C and SIGNALS REF PULSE.

h. Insert card assembly 547955 into test jack J1.

i. Press the ENERGIZE switch on.

j. Readjust the REF PULSE AMPLITUDE control for a 2-volt output.

k. Readjust the REF PULSE DURATION control for a 4-μsec pulse width.

l. Set S1, on card assembly, to 0–.5K position. Set R1, on card assembly, fully counterclockwise.

m. Set S2, on card assembly, to the NORM position. Set S3, on card assembly, to the 1.2 position.

n. Observe positive, 4-μsec, 5-kc pulses at jacks $\overline{T}$ and $\overline{W}$. Observe that adjustment of R18 varies the amplitude of the pulses from 1 to 5 volts.

o. Observe positive, 4-μsec, 5–kc pulses at jack $\overline{E}$. Observe that adjustment of R18 varies the amplitude of the pulses from .5 to 3 volts.

p. Set TRUE-FALSE switch S to the neutral position.

q. Connect a load between jacks S and DC VOLTAGES −28 with jumper leads, and set the LOAD selector switch to position 1.

r. Observe no output signal at jacks $\overline{E}$, $\overline{T}$, and $\overline{W}$.

s. Set TRUE-FALSE switch $\overline{H}$ to the neutral position.

t. Connect a jumper lead between jacks S and $\overline{H}$.

u. Remove the jumper lead from jack C and connect to jack $\overline{K}$.

v. Observe positive, 4-μsec, 5–kc pulses at jacks $\overline{T}$ and $\overline{W}$. Observe that adjustment of R11 varies the amplitude of the pulses from .5 to 5 volts.

w. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

x. Remove all jumper leads from the jacks.

y. Return all TRUE-FALSE switches to the neutral positions.

z. Remove the card assembly from the test jack.

aa. Return all switches and controls to the pretest positions.

53. HFR 1/HFR 2 Video Amplifier Card Assembly 547957

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Press VOLTAGES switch 28 on.

b. Press SELECT switch 5 on.

c. Set TRUE-FALSE switches M, S, X, Y, $\overline{F}$, and $\overline{H}$ to TRUE and $\overline{B}$ to FALSE.

d. Set the AC VAR FREQUENCY switch to VAR and adjust the AC VAR FREQUENCY control for a 5-kc output.

e. Set the REF PULSE AMPLITUDE switch to + and adjust the REF PULSE AMPLITUDE control for a 2-volt output.

f. Set the REF PULSE DURATION switch to SHORT, and adjust the REF PULSE DURATION control for a 4-μsec pulse width.

g. Connect a jumper lead between jack C and SIGNALS REF PULSE.

h. Insert card assembly 547957 into test jack J1.

i. Adjust REFLECTION ADJ R1, control located on card assembly, fully C. W.

j. Press ENERGIZE switch on.

k. Readjust REF PULSE AMPLITUDE control for a 2-volt output.

l. Readjust REF PULSE DURATION control for a 4-μsec pulse width.

m. Set S1 EQUALIZATION on card assembly, to 0–0.5K position.

n. Observe that the 0–85 percent rise time of the positive 4-μsec, 5–KC pulse is less than 1 μsec as measured at $\overline{W}$, TPB1–3, and TPB1–4.

o. Set S1 EQUALIZATION on card assembly to 0.5–2K position.

p. Observe that the 0–85 percent rise time of the positive 4-μsec, 5–KC pulse is less than 0.5 μsec as measured at $\overline{W}$.

q. Set S1 EQUALIZATION on card assembly to 2–3K position.

r. Observe that the 0–85 percent rise time of the positive 4-μsec, 5–KC pulse is less that 0.25 μsec as measured at $\overline{W}$.

s. Observe that adjustment of LIVE VIDEO GAIN R13, located on card assembly, varies the amplitude of the pulses at jack $\overline{W}$ from 1.5 to 5.5 volts.

t. Adjust LIVE VIDEO GAIN R13, located on card assembly fully C.W.

u. Readjust REFLECTION ADJ R1 control CCW, observe that pulse at jack $\overline{W}$ increases 4 volts in amplitude.

v. Observe a negative going 4-volt, 5–KC pulse at a level of +16 volts at TPB1–2.

w. Set TRUE-FALSE switch S to neutral.

x. Connect a load between jack S and DC VOLTAGES −28 with jumper leads, set LOAD switch to position 1.

y. Observe that pulse at jack $\overline{W}$ is not present.

z. Set TRUE-FALSE switch $\overline{H}$ to neutral.

aa. Remove jumper lead from jack S and connect to jack $\overline{H}$.

ab. Set TRUE-FALSE switch S to TRUE.

ac. Remove jumper lead from jack C and connect to jack $\overline{K}$.

ad. Observe positive 4-μsec, 5–KC pulse at jack $\overline{W}$.

ae. Observe that adjustment of SIMULATED HF VIDEO R7 control varies the amplitude of the pulses at jack $\overline{W}$ from 0 to 6 volts ±0.5 volts.

af. Observe that pulses at TPB1–1 correspond to the input pulses.

ag. Remove jumper lead from jack $\overline{H}$, observe that pulse at jack $\overline{W}$ is not present.

ah. Remove all jumper leads from the jacks.

ai. Return all TRUE-FALSE switches to the neutral positions.

aj. Remove the card assembly from the test jack.

ak. Return all switches and controls to the pretest positions.

54. Matrix Card Assembly 548000

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches H, J, R, S, X, $\overline{H}$, J, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548000 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R X		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
II		H		
	1	t	V	0
	2	f	V	−6
III		H X $\overline{H}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
IV		H $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
V		R S H J		
	1	t t t t	C	0
	2	f t t t	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		H S $\overline{H}$ $\overline{J}$		
	1	t t t t	E	0
	2	f t t t	E	−6
	3	t f t t	E	−6
	4	t t f t	E	−6
	5	t t t f	E	−6
VII		R S $\overline{J}$ $\overline{R}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
VIII		H S $\overline{J}$ $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IX		J R $\overline{H}$ $\overline{J}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		H J $\overline{H}$ $\overline{J}$		
	1	t t t t	$\overline{E}$	0
	2	f t t t	$\overline{E}$	−6
	3	t f t t	$\overline{E}$	−6
	4	t t f t	$\overline{E}$	−6
	5	t t t f	$\overline{E}$	−6
XI		J R $\overline{J}$ $\overline{R}$		
	1	t t t t	$\overline{U}$	0
	2	f t t t	$\overline{U}$	−6
	3	t f t t	$\overline{U}$	−6
	4	t t f t	$\overline{U}$	−6
	5	t t t f	$\overline{U}$	−6
XII		H J $\overline{J}$ $\overline{R}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

55. Matrix Card Assembly 548001

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches H, J, R, S, X, $\overline{H}$, $\overline{J}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548001 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H S X $\overline{R}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
II		H J $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		H J X $\overline{J}$ $\overline{R}$		
	1	t t t t t	$\overline{V}$	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
IV		H J $\overline{R}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		R S $\overline{H}$ $\overline{S}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		H S $\overline{H}$ $\overline{S}$		
	1	t t t t	E	0
	2	f t t t	E	−6
	3	t f t t	E	−6
	4	t t f t	E	−6
	5	t t t f	E	−6
VII		R S $\overline{R}$ $\overline{S}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
VIII		H S $\overline{R}$ $\overline{S}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IX		J R $\overline{H}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		H J $\overline{H}$ $\overline{S}$		
	1	t t t t	$\overline{E}$	0
	2	f t t t	$\overline{E}$	−6
	3	t f t t	$\overline{E}$	−6
	4	t t f t	$\overline{E}$	−6
	5	t t t f	$\overline{E}$	−6
XI		J R $\overline{R}$ $\overline{S}$		
	1	t t t t	$\overline{U}$	0
	2	f t t t	$\overline{U}$	−6
	3	t f t t	$\overline{U}$	−6
	4	t t f t	$\overline{U}$	−6
	5	t t t f	$\overline{U}$	−6
XII		H J $\overline{R}$ $\overline{S}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

56. Matrix Card Assembly 548002

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, L, N, S, U, X, Y, $\overline{A}$, $\overline{B}$, $\overline{E}$, J, $\overline{K}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548002 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		U $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		U $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
III		N Y		
	1	t t	V, W, $\overline{C}$	0
	2	f t	V, W, $\overline{C}$	−6
	3	t f	V, W, $\overline{C}$	−6
IV		E U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
V		F U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VI		U $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		U $\overline{U}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		U X $\overline{P}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IX		U X $\overline{E}$ $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
X		S Y $\overline{A}$ J		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XI		N $\overline{B}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		$\overline{B}$ J $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		L $\overline{B}$ $\overline{J}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIV		$\overline{B}$ J $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

57. Matrix Card Assembly 548003

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, L, N, P, U, X, Y, $\overline{A}$, $\overline{E}$, J, $\overline{K}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548003 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		U X $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
II		U X $\overline{E}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
III		$\overline{L}$ P Y J		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IV		N Y		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		Y J $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		Y J $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		Y $\overline{A}$ J		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		E U X $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		F U X $\overline{E}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
X		H Y J $\overline{L}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XI		N Y		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XII		Y J $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		L Y $\overline{J}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		Y $\overline{A}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all the TRUE-FALSE switches to the neutral positions.

i. Measure 10,000 ohms between jacks $\overline{F}$ and $\overline{Y}$.

j. Set AC VAR FREQUENCY switch to 1KC.

k. Press REF PULSE on.

l. Synchronize the oscilloscope for a positive signal at the SYNC SIGNAL connector.

m. Set REF PULSE DURATION switch to LONG, adjust REF PULSE DURATION control for 500 μsec pulse width.

n. Set REF PULSE AMPL switch to +, adjust REF PULSE AMPL control for 7 volts.

o. Set TRUE-FALSE switch $\overline{T}$ to TRUE.

p. Connect a load between jack $\overline{N}$ and SIGNALS REF PULSE. Set the load selector to position 8.

q. Observe that the rising waveform reaches the 6 volt level after 30 to 50 μsec.

r. Remove the matrix assembly from the test jack.

58. Matrix Card Assembly 548004

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, L, N, R, U, X, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548004 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
II		J U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
III		N Y		
	1	t t	V, $\overline{C}$	0
	2	f t	V, $\overline{C}$	−6
	3	t f	V, $\overline{C}$	−6
IV		H U X $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		J U X $\overline{E}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		Y $\overline{F}$ J $\overline{K}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VII		L Y $\overline{J}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		Y J $\overline{L}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		Y $\overline{A}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		E N Y		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		N Z $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		N R Y $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
XIII		F N Z		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to the neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks F, S, and $\overline{R}$.

j. Remove the matrix assembly from the test jack.

59. Matrix Card Assembly 548005

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, E, H, J, K, M, N, P, R, S, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548005 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H N R Y J		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
II		N Z $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		U X $\overline{E}$ F[a]		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IV		J P $\overline{A}$ $\overline{K}$[b]		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
V		P $\overline{B}$ $\overline{K}$ $\overline{P}$[b]		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		E P $\overline{N}$ $\overline{U}$[b]		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VII		K $\overline{R}$ $\overline{U}$ $\overline{X}$[b]		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		$\overline{M}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IX		P $\overline{K}$ $\overline{M}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		B M S		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

[a] Set TRUE-FALSE switches P, $\overline{B}$, $\overline{K}$, and $\overline{P}$ to TRUE for test III.

[b] Set TRUE-FALSE switches U, X, $\overline{E}$, and $\overline{F}$ to TRUE for test IV through VII.

g. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to the neutral positions.

i. Set the AC VAR FREQUENCY switch to 1 KC.

j. Press the REF PULSE switch on.

k. Synchronize the oscilloscope for a negative signal to the SYNC SIGNAL connector.

l. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

m. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

n. Set TRUE-FALSE switch L to TRUE.

o. Connect a load between the L and SIGNALS REF PULSE jacks with jumper leads, and set the LOAD selector switch to position 8.

p. Press the ENERGIZE switch on.

q. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack $\overline{L}$ is 32 to 48 microseconds.

r. Press ENERGIZE switch off.

s. Remove all jumper leads from the jacks.

t. Return all TRUE-FALSE switches to their neutral positions.

u. Measure 10,000 ohms between jack $\overline{Y}$ and jacks $\overline{H}$, $\overline{S}$, and $\overline{T}$.

v. Remove the matrix assembly from the test jack.

w. Return all switches and controls to their pretest positions.

60. Matrix Card Assembly 548006

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, N, P, R, T, U, X, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548006 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		U X $\overline{E}$ $\overline{F}$[a]		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
II		P $\overline{K}$ $\overline{P}$[b]		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
III		E K $\overline{K}$[b]		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IV		P $\overline{R}$ $\overline{U}$[b]		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		F K $\overline{U}$[b]		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		$\overline{M}$		
	1	t	W	0
	2	f	W	−6
VII		N R T $\overline{B}$ J $\overline{S}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
VIII		J N Z		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		H K $\overline{K}$ $\overline{M}$		
	1	t t t t	$\overline{A}$	0
	2	f t t t	$\overline{A}$	−6
	3	t f t t	$\overline{A}$	−6
	4	t t f t	$\overline{A}$	−6
	5	t t t f	$\overline{A}$	−6
X		H P $\overline{K}$ $\overline{M}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XI		H K $\overline{M}$ $\overline{U}$		
	1	t t t t	Y	0
	2	f t t t	Y	−6
	3	t f t t	Y	−6
	4	t t f t	Y	−6
	5	t t t f	Y	−6
XII		H P $\overline{M}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

[a] Set TRUE-FALSE switches E, K, and $\overline{K}$ to TRUE for test I.

[b] Set TRUE-FALSE switches U, X, $\overline{E}$, and $\overline{F}$ to TRUE for tests II through V.

g. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

h. Set the AC VAR FREQUENCY switch to 1 KC.

i. Press the REF PULSE switch on.

j. Synchronize the oscilloscope with a negative signal at the SYNC SIGNAL connector.

k. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6 volt output.

l. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

m. Set TRUE-FALSE switches $\overline{W}$, $\overline{V}$ and $\overline{H}$ to TRUE.

n. Connect a load between jack L and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 8.

o. Press the ENERGIZE switch on.

p. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack L is 32 to 48 microseconds.

q. Remove the jumper lead from jack L and connect it to jack $\overline{L}$.

r. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack $\overline{L}$ is 32 to 48 microseconds.

s. Remove the jumper lead from jack $\overline{L}$ and connect it to jack M.

t. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack Y is 32 to 48 microseconds.

u. Press ENERGIZE switch off.

v. Remove all jumper leads from the jacks.

w. Return all TRUE-FALSE switches to their neutral positions.

x. Measure 10,000 ohms between jack $\overline{Y}$ and jacks J and S.

y. Remove the matrix assembly from the test jack.

z. Return all switches and controls to their pretest positions.

61. Matrix Card Assembly 548007

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, X, $\overline{E}$, $\overline{F}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548007 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H P $\overline{P}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		L		
	1	t	V,$\overline{C}$,$\overline{D}$	0
	2	f	V,$\overline{C}$,$\overline{D}$	−6
III		E F J R $\overline{E}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		S $\overline{F}$ $\overline{R}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
V		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VI		N		
	1	t	D	0
	2	f	D	−6
VII		X		
	1	t	W	0
	2	f	W	−6

g. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to the neutral positions.

i. Measure 10,0000 ohms between jacks $\overline{Y}$ and $\overline{P}$.

j. Remove the matrix assembly from the test jack.

62. Matrix Card Assembly 548008

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548008 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E H J N S U $\overline{F}$ $\overline{H}$ $\overline{L}$ $\overline{P}$		
	1	t t t t t t t t t t	W	0
	2	f t t t t t t t t t	W	−6
	3	t f t t t t t t t t	W	−6
	4	t t f t t t t t t t	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	5	t t t f t t t t t t	W	−6
	6	t t t t f t t t t t	W	−6
	7	t t t t t f t t t t	W	−6
	8	t t t t t t f t t t	W	−6
	9	t t t t t t t f t t	W	−6
	10	t t t t t t t t f t	W	−6
	11	t t t t t t t t t f	W	−6
II		E P R S T $\overline{E}$ F J $\overline{K}$ U		
	1	t t t t t t t t t t	W	0
	2	f t t t t t t t t t	W	−6
	3	t f t t t t t t t t	W	−6
	4	t t f t t t t t t t	W	−6
	5	t t t f t t t t t t	W	−6
	6	t t t t f t t t t t	W	−6
	7	t t t t t f t t t t	W	−6
	8	t t t t t t f t t t	W	−6
	9	t t t t t t t f t t	W	−6
	10	t t t t t t t t f t	W	−6
	11	t t t t t t t t t f	W	−6
III		F X $\overline{B}$ T		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		$\overline{A}$ $\overline{R}^a$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
V		K Z^a		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		Y $\overline{S}^a$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		$\overline{M}$ $\overline{N}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		L		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

[a] Set TRUE-FALSE switches X and $\overline{T}$ to TRUE for tests IV, V, and VI.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

63. Matrix Card Assembly 548009

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, T, U, X, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548009 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H $\overline{N}$ $\overline{T}$[a]		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		T[b]		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
III		U[b]		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
IV		K[b]		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
V		X		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		L		
	1	t	C	0
	2	f	C	−6
VII		K X $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		E K X		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		F J L		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
X		J L $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XI		K P		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XII		K N $\overline{R}$		
	1	t t t	W	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XIII		E K N R		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6

[a] Set TRUE-FALSE switch T to TRUE.
[b] Set TRUE-FALSE switches H, $\overline{N}$, and $\overline{T}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks E, F, T, $\overline{P}$, and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

64. Matrix Card Assembly 548010

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, P, R, S, X, $\overline{F}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548010 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F X $\overline{T}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		L		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		L R		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IV		J L		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		E H P $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VI		E H K		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VII		X		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VIII		S X $\overline{F}$ $\overline{T}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IX		F X $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks F, J, R, and $\overline{F}$.

j. Remove the matrix assembly from the test jack.

65. Matrix Card Assembly 548011

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, J, K, L, N, P, R, S, T, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548011 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		T $\overline{E}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
II		K P S $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		F K R		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		N		
	1	t	C, $\overline{W}$	0
	2	f	C, $\overline{W}$	−6
V		J L		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		J $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		E $\overline{H}$ $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		E $\overline{E}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks K and E.

j. Remove the matrix assembly from the test jack.

66. Matrix Card Assembly 548012

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches C, D, E, F, H, J, L, M, N, P, R, S, T, U, V, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548012 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F P T		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		E F H		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		U $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		L M Y J $\overline{S}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
V		$\overline{E}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		N $\overline{H}$ $\overline{V}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		L M V J $\overline{P}$ $\overline{S}$		
	1	t t t t t t	$\overline{D}$	0
	2	f t t t t t	$\overline{D}$	−6
	3	t f t t t t	$\overline{D}$	−6
	4	t t f t t t	$\overline{D}$	−6
	5	t t t f t t	$\overline{D}$	−6
	6	t t t t f t	$\overline{D}$	−6
	7	t t t t t f	$\overline{D}$	−6
VIII		D J $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		N Z $\overline{B}$ $\overline{V}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		N R Z $\overline{V}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		X		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XII		C		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XIII		D S J $\overline{K}$ $\overline{T}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XIV		$\overline{A}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

67. Matrix Card Assembly 548014

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches H, K, L, M, N, P, R, S, T, U, $\overline{A}$, $\overline{C}$, $\overline{D}$, F, $\overline{H}$, J, $\overline{M}$, $\overline{N}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548014 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
II		T $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
III		$\overline{R}$ T		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IV		H $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
V		$\overline{N}$ $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VI		$\overline{M}$ $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		R $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		H $\overline{D}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		H $\overline{F}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		H J		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XI		H $\overline{A}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XII		H $\overline{C}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIII		H N		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIV		H U		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XV		H S		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVI		H P		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVII		H M		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVIII		H K		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

68. Matrix Card Assembly 548016

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches H, J, R, S, U, V, X, Y, H, J, K, L, M, P, R, T, U, and W to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548016 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P U		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
II		L U		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
III		H U		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IV		K M		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
V		R		
	1	t	D	0
	2	f	D	−6
VI		U		
	1	t	D	0
	2	f	D	−6
VII		Y		
	1	t	D	0
	2	f	D	−6
VIII		X		
	1	t	D	0
	2	f	D	−6
IX		R		
	1	t	E	0
	2	f	E	−6
X		H		
	1	t	W	0
	2	f	W	−6
XI		V J		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XII		S W		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIII		J T		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XIV		J S		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{F}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

69. Matrix Card Assembly 548018

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, K, L, N, R, U, V, X, Y, Z, J, $\overline{K}$, $\overline{N}$, $\overline{P}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548018 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Z J $\overline{K}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		L V[a]		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
III		F $\overline{T}$[a]		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		R[b]		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
V		$\overline{N}$[b]		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		N[b]		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VII		E Y		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		K Y		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		E X		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
X		U		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

[a] Set TRUE-FALSE switch R to TRUE.
[b] Set TRUE-FALSE switches L and V to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

70. Matrix Card Assembly 548020

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, J, K, L, M, P, R, U, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548020 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		U J $\overline{T}$		
	1	t t t	D, $\overline{W}$	0
	2	f t t	D, $\overline{W}$	−6
	3	t f t	D, $\overline{W}$	−6
	4	t t f	D, $\overline{W}$	−6
II		$\overline{E}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		F P		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IV		E $\overline{N}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		$\overline{M}$		
	1	t	V	0
	2	f	V	−6
VI		Y Z $\overline{F}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		L M X J $\overline{S}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
VIII		$\overline{E}$ $\overline{U}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IX		Z $\overline{F}$ $\overline{P}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
X		K L M R $\overline{J}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
XI		J $\overline{B}$ $\overline{H}$ $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XII		L $\overline{E}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIII		$\overline{K}$		
	1	t	W	0
	2	f	W	−6
XIV		J $\overline{F}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

71. Matrix Card Assembly 548022

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches D, J, K, L, M, R, S, V, Z, $\overline{F}$, $\overline{H}$, J, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks U and DC

VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548022 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L J $\overline{P}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
II		Z $\overline{W}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
III		M $\overline{W}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IV		$\overline{F}$ $\overline{W}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		$\overline{H}$ $\overline{W}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VI		J L M $\overline{F}$ $\overline{S}$		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6
VII		D Z		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		D $\overline{P}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		D $\overline{J}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		D $\overline{H}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XI		S $\overline{R}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
XII		V $\overline{R}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
XIII		K $\overline{R}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks R and $\overline{Y}$.

l. Remove the matrix assembly from the test jack.

72. Matrix Card Assembly 548024

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, P, R, S, T, Y, Z, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks U and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8. Connect LOAD 2 between jacks E and DC VOLTAGES −50 with jumper leads, and set the corresponding LOAD selector switch to position 8.

e. Insert matrix assembly 548024 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K L Y $\overline{F}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
II		K R Z		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
III		K R $\overline{J}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IV		F		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
V		J Z $\overline{F}$ $\overline{S}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		L $\overline{B}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		$\overline{B}$ $\overline{J}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		$\overline{B}$ $\overline{H}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		H P $\overline{N}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
X		E T $\overline{N}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
XI		K M Z $\overline{J}$ $\overline{M}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
XII		S $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIII		K $\overline{F}$ $\overline{M}$ $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		S $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XV		D $\overline{R}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

73. Matrix Card Assembly 548027

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches B, H, K, P, $\overline{A}$, $\overline{D}$, $\overline{F}$, $\overline{K}$, $\overline{M}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548027 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		B $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		K $\overline{M}$ $\overline{T}$ $\overline{U}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		K $\overline{K}$ $\overline{M}$ $\overline{T}$		
	1	t t t t	$\overline{B}$	0
	2	f t t t	$\overline{B}$	−6
	3	t f t t	$\overline{B}$	−6
	4	t t f t	$\overline{B}$	−6
	5	t t t f	$\overline{B}$	−6
IV		B $\overline{A}$ $\overline{D}$		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6
V		P $\overline{M}$ $\overline{T}$ $\overline{U}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		B H $\overline{A}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Set the AC VAR FREQUENCY switch to 1 KC.

j. Press the REF PULSE SWITCH on.

k. Synchronize the oscilloscope for a negative signal at the SYNC SIGNAL connector.

l. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a 6-volt output.

m. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

n. Set TRUE-FALSE switches F, T, and $\overline{R}$ to TRUE.

o. Connect a load between jack S and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 8.

p. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack S is 30 to 50-μsec.

q. Remove the load jumper lead from jack S and connect it to jack $\overline{\text{N}}$.

r. Observe that the 0 to 65 percent rise time of the negative-going waveform at jack $\overline{\text{N}}$ is 30 to 50-μsec.

s. Remove the load jumper lead from jack $\overline{\text{N}}$ and connect it to jack P.

t. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack P is 30 to 50-μsec.

u. Remove the matrix assembly from the test jack.

74. Matrix Card Assembly 548039

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches H, J, K, R, S, Z, $\overline{\text{H}}$, J, $\overline{\text{R}}$, and $\overline{\text{S}}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548039 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J		
	1	t	V	0
	2	f	V	−6
II		H J $\overline{\text{R}}$ $\overline{\text{S}}$		
	1	t t t t	X	0
	2	f t t t	X	−6
	3	t f t t	X	−6
	4	t t f t	X	−6
	5	t t t f	X	−6
III		H J $\overline{\text{S}}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IV		J $\overline{\text{J}}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		Z		
	1	t	W	0
	2	f	W	−6
VI		H J $\overline{\text{H}}$ $\overline{\text{S}}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
VII		Z		
	1	t	E	0
	2	f	E	−6
VIII		J S $\overline{\text{S}}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IX		K R		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		J $\overline{\text{S}}$		
	1	t t	$\overline{\text{C}}$	0
	2	f t	$\overline{\text{C}}$	−6
	3	t f	$\overline{\text{C}}$	−6
XI		H		
	1	t	$\overline{\text{D}}$	0
	2	f	$\overline{\text{D}}$	−6
XII		H J $\overline{\text{R}}$ $\overline{\text{S}}$		
	1	t t t t	$\overline{\text{B}}$	0
	2	f t t t	$\overline{\text{B}}$	−6
	3	t f t t	$\overline{\text{B}}$	−6
	4	t t f t	$\overline{\text{B}}$	−6
	5	t t t f	$\overline{\text{B}}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

75. Matrix Card Assembly 548041

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, L, N, R, T, Y, Z, $\overline{H}$, J, $\overline{L}$, P, R, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks M and DC VOLTAGES 50 with jumper leads and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548041 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Z		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
II		L		
	1	t	D	0
	2	f	D	−6
III		H J $\overline{H}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IV		N R J		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
V		$\overline{P}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
VI		$\overline{S}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VII		H $\overline{H}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VIII		J $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IX		$\overline{U}$		
	1	t	K	0
	2	f	K	−6
X		N $\overline{S}$		
	1	t t	K	0
	2	f t	K	−6
	3	t f	K	−6
XI		T Y		
	1	t t	L–15[a]	0
	2	f t	L–15[a]	−6
	3	t f	L–15[a]	−6
XII		$\overline{L}$		
	1	t	P–25[a]	0
	2	f	P–25[a]	−6

[a] This test point is on the matrix assembly.

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Set the AC VAR FREQUENCY switch to 1 KC.

l. Press the REF PULSE switch on.

m. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

n. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

o. Set the REF PULSE DURATION switch to

LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

p. Connect a jumper between L15 on the card assembly and test jack GRD.

q. Connect a load between jack $\overline{N}$ and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 8.

r. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack $\overline{N}$ is 20 to 45-μsec.

s. Remove the jumper lead from L15 and connect to P25 on the card assembly.

t. Observe that the 0 to 85 percent rise time of the negative-going waveform at jack $\overline{N}$ is 20 to 40-μsec.

u. Remove the matrix assembly from the test jack.

76. Matrix Card Assembly 548042

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548042 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L Y		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		Y $\overline{U}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
III		E F R Z		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		E F J $\overline{B}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		$\overline{A}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		F P Z $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		F N P $\overline{B}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		H $\overline{A}$ $\overline{R}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
IX		H K $\overline{C}$ $\overline{P}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
X		H X $\overline{N}$ $\overline{P}$ $\overline{V}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks E and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

77. Matrix Card Assembly 548043

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, K, M, N, P, R, S, T, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548043 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K		
	1	t	C	0
	2	f	C	−6
II		J		
	1	t	E	0
	2	f	E	−6
III		H		
	1	t	F	0
	2	f	F	−6
IV		T		
	1	t	U	0
	2	f	U	−6
V		S		
	1	t	V	0
	2	f	V	−6
VI		R		
	1	t	W	0
	2	f	W	−6
VII		P		
	1	t	X	0
	2	f	X	−6
VIII		N		
	1	t	Y	0
	2	f	Y	−6
IX		$\overline{F}$		
	1	t	$\overline{A}$	0
	2	f	$\overline{A}$	−6
X		$\overline{K}$		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
XI		$\overline{J}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XII		$\overline{H}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XIII		M		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
XIV		$\overline{R}$		
	1	t	$\overline{T}$	0
	2	f	$\overline{T}$	−6
XV		$\overline{S}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XVI		$\overline{P}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XVII		$\overline{N}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between $\overline{Y}$ and H, $\overline{Y}$ and J, $\overline{Y}$ and R, $\overline{Y}$ and S, $\overline{Y}$ and J, and $\overline{Y}$ and $\overline{S}$.

j. Remove the matrix assembly from the test jack.

78. Matrix Card Assembly 548069

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches D, E, F, J, K, L, M, N, P, S, T, U, Z, $\overline{A}$, $\overline{C}$, $\overline{D}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548069 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S[a]		
	1	t	W	0
	2	f	W	−6
II		$\overline{A}$[a]		
	1	t	W	0
	2	f	W	−6
III		$\overline{P}$[a]		
	1	t	W	0
	2	f	W	−6
IV		$\overline{K}$[a]		
	1	t	W	0
	2	f	W	−6
V		U[a]		
	1	t	W	0
	2	f	W	−6
VI		$\overline{T}$[a]		
	1	t	W	0
	2	f	W	−6
VII		$\overline{C}$[b]		
	1	t	W	0
	2	f	W	−6
VIII		N[b]		
	1	t	W	0
	2	f	W	−6
IX		$\overline{L}$[b]		
	1	t	W	0
	2	f	W	−6
X		U[b]		
	1	t	W	0
	2	f	W	−6
XI		D[c]		
	1	t	W	0
	2	f	W	−6
XII		U[c]		
	1	t	W	0
	2	f	W	−6
XIII		Z $\overline{N}$ $\overline{U}$[c]		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XIV		P $\overline{D}$ $\overline{M}$[c]		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XV		$\overline{R}$[c]		
	1	t	W	0
	2	f	W	−6
XVI		$\overline{H}$[d]		
	1	t	W	0
	2	f	W	−6
XVII		L[d]		
	1	t	W	0
	2	f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVIII		E J[d]		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIX		F J[d]		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XX		K M[d]		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XXI		U[d]		
	1	t	W	0
	2	f	W	−6

[a] Set TRUE-FALSE switches D, L, and T to TRUE.
[b] Set TRUE-FALSE switches D, L, and S to TRUE.
[c] Set TRUE-FALSE switches L, S, and T to TRUE.
[d] Set TRUE-FALSE switches D, S, and T to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

79. Matrix Card Assembly 548071

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches C, E, H, J, K, L, M, N, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548071 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		X Z $\overline{J}$ $\overline{S}$ $\overline{U}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
II		T $\overline{T}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
III		$\overline{A}$ $\overline{H}$ $\overline{M}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IV		Y $\overline{H}$ $\overline{M}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
V		$\overline{H}$ $\overline{K}$ $\overline{M}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VII		$\overline{D}$ $\overline{R}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f		
VII		U		
	1	t	V, $\overline{C}$	0
	2	f	V, $\overline{C}$	−6
VIII		M S X Z $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IX		K L T		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		J L $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		E M $\overline{A}$ $\overline{H}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XII		E M Y $\overline{H}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XIII		E M $\overline{H}$ $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XIV		$\overline{E}$ $\overline{R}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XV		H Z		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XVI		C N Z		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

80. Matrix Card Assembly 548072

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, E, F, H, K, L, M, N, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548072 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K $\overline{B}$ $\overline{E}$ J		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
II		M $\overline{B}$ $\overline{E}$ $\overline{L}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		N $\overline{B}$ $\overline{E}$ $\overline{T}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IV		B L $\overline{B}$ $\overline{E}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
V		T Z		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		Y $\overline{P}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		H S $\overline{A}$ $\overline{K}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VIII		H R $\overline{A}$ $\overline{K}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		H X $\overline{A}$ $\overline{K}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
X		T		
	1	t	V, $\overline{C}$	0
	2	f	V, $\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		F $\overline{F}$ $\overline{M}$ $\overline{N}$ $\overline{S}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
XII		F $\overline{E}$ $\overline{H}$ $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
XIII		T U		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIV		E T		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks E, P, $\overline{K}$, and $\overline{U}$.

j. Remove all jumper leads from the jacks.

k. Remove the matrix assembly from the test jack.

81. Matrix Card Assembly 548073

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, K, L, M, N, P, R, S, X, Z, $\overline{A}$, $\overline{H}$, J, $\overline{L}$, $\overline{N}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548073 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used

in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P S $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		N Z		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		E L R $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		E F M N		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		E H R X		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		E F K X		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		E R $\overline{H}$ $\overline{N}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		P $\overline{J}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		E F $\overline{N}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		E R X $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		E F X $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

82. Matrix Card Assembly 548074

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, N, P, R, S, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548074 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used

in each test to FALSE before proceeding to the vext test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S U Y $\overline{F}$ $\overline{N}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
II		P S U Z $\overline{F}$ $\overline{N}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
III		R U $\overline{B}$ $\overline{F}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		R U $\overline{A}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		J $\overline{P}$		
	1	t t	V, W	0
	2	f t	V, W	−6
	3	t f	V, W	−6
VI		K S U Z $\overline{N}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VII		K R U $\overline{H}$ $\overline{S}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
VIII		H N J $\overline{L}$		
	1	t t t t	E	0
	2	f t t t	E	−6
	3	t f t t	E	−6
	4	t t f t	E	−6
	5	t t t f	E	−6
IX		J L $\overline{E}$ $\overline{K}$ $\overline{M}$		
	1	t t t t t	X	0
	2	f t t t t	X	−6
	3	t f t t t	X	−6
	4	t t f t t	X	−6
	5	t t t f t	X	−6
	6	t t t t f	X	−6
X		F		
	1	t	X	0
	2	f	X	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks T and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

83. Matrix Card Assembly 548076

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches H, J, K, P, R, S, U, V, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548076 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used

in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S U Z $\overline{N}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		R U V $\overline{B}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
III		J $\overline{P}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		U X Y $\overline{F}$ $\overline{N}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
V		U V $\overline{R}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
VI		U X Z $\overline{F}$ $\overline{N}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VII		R U V $\overline{A}$ $\overline{F}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VIII		P U Z $\overline{H}$ $\overline{N}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
IX		K U Z $\overline{N}$ $\overline{T}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
X		J $\overline{P}$		
	1	t t	W, $\overline{E}$	0
	2	f t	W, $\overline{E}$	−6
	3	t f	W, $\overline{E}$	−6
XI		H U V		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks H and $\overline{R}$.

j. Remove the matrix assembly from the test jack.

84. Matrix Card Assembly 548078

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, P, R, S, T, U, X, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548078 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K R U $\overline{S}$ $\overline{T}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
II		S U $\overline{A}$ $\overline{B}$ $\overline{L}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
III		J $\overline{P}$		
	1	t t	W, $\overline{C}$	0
	2	f t	W, $\overline{C}$	−6
	3	t f	W, $\overline{C}$	−6
IV		P R T U $\overline{F}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t	C	0
	2	f t t t t t t	C	−6
	3	t f t t t t t	C	−6
	4	t t f t t t t	C	−6
	5	t t t f t t t	C	−6
	6	t t t t f t t	C	−6
	7	t t t t t f t	C	−6
	8	t t t t t t f	C	−6
V		S U Z $\overline{B}$ $\overline{L}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VI		H J L $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VII		H J $\overline{R}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		F		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IX		X $\overline{H}$ J $\overline{K}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
X		X $\overline{E}$ $\overline{H}$ $\overline{K}$ $\overline{R}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
XI		J		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks H, L, and $\overline{L}$.

j. Remove the matrix assembly from the test jack.

85. Matrix Card Assembly 548082

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches H, K, L, S, T, X, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{F}$, J, $\overline{K}$, $\overline{P}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548082 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H $\overline{C}$ $\overline{P}$ $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
II		H K X $\overline{P}$ $\overline{V}$		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6
III		L X		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IV		S Z $\overline{C}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		K T X $\overline{P}$ $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VI		Z $\overline{C}$ J		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		H Z $\overline{C}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		L X		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		X $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
X		T $\overline{C}$ $\overline{P}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		X $\overline{A}$ J		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		H X $\overline{A}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		X Z $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		$\overline{B}$[a]		
	1	t	L	0
	2	f	L	−6

[a] Set TRUE-FALSE switch L to neutral position.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

86. Matrix Card Assembly 548085

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches C, D, E, F, N, W, $\overline{C}$, $\overline{D}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548085 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
II		$\overline{W}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
III		W		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
IV		E		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
V		$\overline{C}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
VI		N		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
VII		F		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
VIII		C		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
IX		D		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
X		E		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
XI		$\overline{C}$		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
XII		$\overline{D}$		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
XIII		F		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XIV		$\overline{W}$		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XV		D		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XVI		E		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVII		$\overline{C}$		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XVIII		$\overline{D}$		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

87. Matrix Card Assembly 548087

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, D, E, F, N, P, T, W, Y, Z, $\overline{C}$, $\overline{D}$, $\overline{F}$, $\overline{P}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548087 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switch settings used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F		
	1	t	J	0
	2	f	J	−6
II		C		
	1	t	J	0
	2	f	J	−6
III		D		
	1	t	J	0
	2	f	J	−6
IV		E		
	1	t	J	0
	2	f	J	−6
V		$\overline{C}$		
	1	t	J	0
	2	f	J	−6
VI		N		
	1	t	J	0
	2	f	J	−6
VII		C P T W Y $\overline{D}$ $\overline{P}$		
	1	t t t t t t t	K	0
	2	f t t t t t t	K	−6
	3	t f t t t t t	K	−6
	4	t t f t t t t	K	−6
	5	t t t f t t t	K	−6
	6	t t t t f t t	K	−6
	7	t t t t t f t	K	−6
	8	t t t t t t f	K	−6
VIII		$\overline{W}$		
	1	t	L	0
	2	f	L	−6
IX		D		
	1	t	L	0
	2	f	L	−6
X		E		
	1	t	L	0
	2	f	L	−6
XI		$\overline{C}$		
	1	t	L	0
	2	f	L	−6
XII		N		
	1	t	L	0
	2	f	L	−6
XIII		$\overline{F}$		
	1	t	L	0
	2	f	L	−6
XIV		Z		
	1	t	L	0
	2	f	L	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

88. Matrix Card Assembly 548089

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, D, E, H, J, K, M, N, P, R, S, T, W, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548089 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P $\overline{A}$ $\overline{B}$ $\overline{M}$ $\overline{P}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
II		P $\overline{C}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		P $\overline{K}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		P $\overline{E}$ J $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		$\overline{U}$ $\overline{V}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		Z		
	1	t	V	0
	2	f	V	−6
VII		E $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		E R $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		E H S		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		E J $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		K R $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		C D T W Y $\overline{D}$ $\overline{W}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6

Test No.	Step No.	TRUE-FALSE stitches	Test point	Output voltage
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
XIII		M N		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

89. Matrix Card Assembly 548091

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches B, E, F, K, L, M, N, P, R, S, U, X, Z, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, and $\overline{P}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548091 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L U $\overline{H}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		U $\overline{B}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		U $\overline{D}$ $\overline{K}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		U $\overline{E}$ $\overline{H}$ $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		N S U $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		E U $\overline{F}$ $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		B P R Z $\overline{M}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		K P $\overline{B}$ $\overline{C}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		P R $\overline{B}$ $\overline{L}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		K P X $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		L P $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		F M P Z $\overline{M}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

90. Matrix Card Assembly 548093

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches B, E, F, H, J, K, L, N, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{C}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548093 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E W $\overline{L}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		E X $\overline{N}$ $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		H X $\overline{C}$ $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		J S U $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		K R U $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		L N U $\overline{M}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		K U Y $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		U Z $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		U $\overline{A}$ J $\overline{N}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
X		P $\overline{P}$ $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		B P Z $\overline{A}$ $\overline{P}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XII		F P T Z $\overline{P}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

91. Matrix Card Assembly 548095

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, H, J, K, L, N, R, S, T, W, X, Y, Z, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548095 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		W Z $\overline{E}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		H J $\overline{M}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		H K L N		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		H K Y $\overline{C}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		H X $\overline{N}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		H L $\overline{H}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		H $\overline{B}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		H $\overline{C}$ $\overline{D}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		H $\overline{K}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		E $\overline{F}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		K R S W $\overline{B}$ $\overline{L}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
XII		K R T W $\overline{B}$ $\overline{L}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

92. Matrix Card Assembly 548117

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, M, N, P, R, S, T, X, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks $\overline{E}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548117 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N S $\overline{H}$ $\overline{L}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		N S $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		N R S $\overline{L}$ $\overline{T}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		B		
	1	t	V	0
	2	f	V	−6
V		$\overline{B}$ $\overline{R}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VI		$\overline{B}$ $\overline{F}$ $\overline{L}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VII		P $\overline{B}$ $\overline{L}$ $\overline{R}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VIII		K $\overline{B}$ $\overline{R}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IX		N T $\overline{K}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
X		N $\overline{J}$		
	1	t t	Y	0
	2	f t	Y	−6
	3	t f	Y	−6
XI		E M $\overline{A}$ $\overline{T}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
XII		L $\overline{M}$ $\overline{N}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
XIII		F H $\overline{M}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
XIV		E J K M X $\overline{H}$ $\overline{P}$ $\overline{R}$		
	1	t t t t t t t t	Z	0
	2	f t t t t t t t	Z	−6
	3	t f t t t t t t	Z	−6
	4	t t f t t t t t	Z	−6
	5	t t t f t t t t	Z	−6
	6	t t t t f t t t	Z	−6
	7	t t t t t f t t	Z	−6
	8	t t t t t t f t	Z	−6
	9	t t t t t t t f	Z	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jack $\overline{Y}$ and jacks J, R, and $\overline{F}$.

l. Remove the matrix assembly from the test jack.

93. Matrix Card Assembly 548119

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548119 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
I		E	T	Y	$\overline{F}$	$\overline{H}$	$\overline{K}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	D	0
	2	f	t	t	t	t	t	t	D	−6
	3	t	f	t	t	t	t	t	D	−6
	4	t	t	f	t	t	t	t	D	−6
	5	t	t	t	f	t	t	t	D	−6
	6	t	t	t	t	f	t	t	D	−6
	7	t	t	t	t	t	f	t	D	−6
	8	t	t	t	t	t	t	f	D	−6
II		P	Y	$\overline{F}$	$\overline{H}$	$\overline{P}$				
	1	t	t	t	t	t			D	0
	2	f	t	t	t	t			D	−6
	3	t	f	t	t	t			D	−6
	4	t	t	f	t	t			D	−6
	5	t	t	t	f	t			D	−6
	6	t	t	t	t	f			D	−6
III		X	$\overline{S}$							
	1	t	t						D	0
	2	f	t						D	−6
	3	t	f						D	−6
IV		H	Y							
	1	t	t						D	0
	2	f	t						D	−6
	3	t	f						D	−6
V		J	Z	$\overline{L}$						
	1	t	t	t					W	0
	2	f	t	t					W	−6
	3	t	f	t					W	−6
	4	t	t	f					W	−6
VI		F	L	R	U	Z	$\overline{A}$	$\overline{E}$	$\overline{W}$		
	1	t	t	t	t	t	t	t	t	W	0
	2	f	t	t	t	t	t	t	t	W	−6
	3	t	f	t	t	t	t	t	t	W	−6
	4	t	t	f	t	t	t	t	t	W	−6
	5	t	t	t	f	t	t	t	t	W	−6
	6	t	t	t	t	f	t	t	t	W	−6
	7	t	t	t	t	t	f	t	t	W	−6
	8	t	t	t	t	t	t	f	t	W	−6
	9	t	t	t	t	t	t	t	f	W	−6
VII		M	Y	$\overline{N}$	$\overline{S}$						
	1	t	t	t	t					W	0
	2	f	t	t	t					W	−6
	3	t	f	t	t					W	−6
	4	t	t	f	t					W	−6
	5	t	t	t	f					W	−6
VIII		R	X								
	1	t	t							W	0
	2	f	t							W	−6
	3	t	f							W	−6
IX		M	Y	$\overline{M}$	$\overline{N}$						
	1	t	t	t	t					W	0
	2	f	t	t	t					W	−6
	3	t	f	t	t					W	−6
	4	t	t	f	t					W	−6
	5	t	t	t	f					W	−6
X		H	Y								
	1	t	t							$\overline{V}$	0
	2	f	t							$\overline{V}$	−6
	3	t	f							$\overline{V}$	−6
XI		S	$\overline{X}$	$\overline{B}$							
	1	t	t	t						$\overline{V}$	0
	2	f	t	t						$\overline{V}$	−6
	3	t	f	t						$\overline{V}$	−6
	4	t	t	f						$\overline{V}$	−6
XII		X	J	$\overline{U}$							
	1	t	t	t						$\overline{V}$	0
	2	f	t	t						$\overline{V}$	−6
	3	t	f	t						$\overline{V}$	−6
	4	t	t	f						$\overline{V}$	−6
XIII		N	S								
	1	t	t							V	0
	2	f	t							V	−6
	3	t	f							V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		N $\overline{J}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XV		N		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack

i. Return all TRUE-FALSE switches to neutral positions.

94. Matrix Card Assembly 548121

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, E, F, H, J, K, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548121 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K L $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		E $\overline{A}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
III		N $\overline{N}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IV		N T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		Z $\overline{S}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VI		E Z $\overline{T}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VII		J M Z $\overline{E}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VIII		Z $\overline{L}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IX		N S		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		N		
	1	t	$\overline{C}$	−0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		M $\overline{A}$ $\overline{E}$ $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XII		H $\overline{A}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIII		B E $\overline{A}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIV		F J M R X Y $\overline{J}$		
	1	t t t t t t t	D	0
	2	f t t t t t t	D	−6
	3	t f t t t t t	D	−6
	4	t t f t t t t	D	−6
	5	t t t f t t t	D	−6
	6	t t t t f t t	D	−6
	7	t t t t t f t	D	−6
	8	t t t t t t f	D	−6
XV		P U Y $\overline{J}$ $\overline{M}$ $\overline{U}$		
	1	t t t t t t	D	0
	2	f t t t t t	D	−6
	3	t f t t t t	D	−6
	4	t t f t t t	D	−6
	5	t t t f t t	D	−6
	6	t t t t f t	D	−6
	7	t t t t t f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

95. Matrix Card Assembly 548122

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, J, K, L, M, N, P, R, S, T, U, $\overline{B}$, $\overline{E}$, $\overline{F}$, H, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548122 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test	Step	TRUE-FALSE									Test	Output age
I		J	K	M	T	$\overline{M}$	$\overline{N}$	$\overline{P}$	$\overline{R}$	$\overline{S}$		
	1	t	t	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	t	t	C	−6
	6	t	t	t	t	f	t	t	t	t	C	−6
	7	t	t	t	t	t	f	t	t	t	C	−6
	8	t	t	t	t	t	t	f	t	t	C	−6
	9	t	t	t	t	t	t	t	f	t	C	−6
	10	t	t	t	t	t	t	t	t	f	C	−6
II		N	P	R	U	$\overline{E}$	$\overline{F}$	$\overline{H}$	$\overline{J}$	$\overline{K}$		
	1	t	t	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	t	t	C	−6
	6	t	t	t	t	f	t	t	t	t	C	−6
	7	t	t	t	t	t	f	t	t	t	C	−6
	8	t	t	t	t	t	t	f	t	t	C	−6
	9	t	t	t	t	t	t	t	f	t	C	−6
	10	t	t	t	t	t	t	t	t	f	C	−6
III		S[a]										
	1	t									C	0
	2	f									C	−6
IV		$\overline{B}$										
	1	t									V	0
	2	f									V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		K L $\overline{H}$ $\overline{L}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VI		K L $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		E		
	1	t	$\overline{T}$	0
	2	f	$\overline{T}$	−6

[a] Set TRUE-FALSE switches N, P, R, U, $\overline{E}$, $\overline{F}$, $\overline{H}$, and $\overline{K}$ to TRUE for test III. Return to FALSE when test is completed.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks K, N, $\overline{H}$, $\overline{P}$, and $\overline{R}$.

j. Remove the matrix assembly from the test jack.

96. Matrix Card Assembly 548123

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, J, L, M, N, P, R, S, X, Y, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks W and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548123 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E M $\overline{A}$ $\overline{H}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
II		X		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
III		$\overline{H}$		
	1	t	V	0
	2	f	V	−6
IV		$\overline{F}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
V		E		
	1	t	D	0
	2	f	D	−6
VI		Y		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
VII		$\overline{N}$		
	1	t	U	0
	2	f	U	−6
VIII		J		
	1	t	Z	0
	2	f	Z	−6
IX		$\overline{T}$		
	1	t	K	0
	2	f	K	−6
X		F		
	1	t	C	0
	2	f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		$\overline{R}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XII		N $\overline{L}$ $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		L $\overline{B}$ $\overline{J}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
XIV		P R $\overline{B}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
XV		Y $\overline{N}$		
	1	t t	H	0
	2	f t	H	−6
	3	t f	H	−6
XVI		J S $\overline{M}$		
	1	t t t	H	0
	2	f t t	H	−6
	3	t f t	H	−6
	4	t t f	H	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jack $\overline{Y}$ and jacks E, F, S, $\overline{H}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, and $\overline{T}$.

l. Remove the matrix assembly from the test jacks.

97. Matrix Card Assembly 548124

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches C, D, E, F, H, J, K, L, M, N, P, R, U, W, X, Y, Z, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548124 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
II		D H P Z $\overline{E}$ $\overline{T}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
III		D P U Z E $\overline{J}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
IV		D F X Y $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		D L X Y $\overline{J}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		N R		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		D M P Y $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		D K P Y J		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IX		$\overline{C}$ $\overline{F}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
X		$\overline{B}$ $\overline{K}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XI		$\overline{H}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XII		$\overline{K}$ $\overline{L}$ $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		W $\overline{K}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIV		$\overline{S}$		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
XV		C E		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

98. Matrix Card Assembly 548126

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches D, F, H, J, K, L, M, N, P, S, U, X, Y, Z, $\overline{A}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548126 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J $\overline{C}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
II		P Z $\overline{E}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		N $\overline{U}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		Y $\overline{S}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
V		J $\overline{F}$ $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VI		H P Z $\overline{E}$ $\overline{T}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VII		D P U Z $\overline{E}$ J		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
VIII		F X Y $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		L X Y J		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Out-4put voltage
X		M P Y $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XI		P S Y J		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XII		K N $\overline{A}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XIII		K N $\overline{M}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XIV		$\overline{P}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XV		$\overline{S}$		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

99. Matrix Card Assembly 548128

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, N, P, R, S, T, U, W, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, H, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548128 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		D		
	1	t	V	0
	2	f	V	−6
II		T W $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		S $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IV		U $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		L W $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		P W $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		H J $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		S W $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		F H W $\overline{A}$ J $\overline{M}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
X		E $\overline{L}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		W $\overline{M}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		K $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIII		W $\overline{H}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		H W $\overline{L}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XV		S W $\overline{M}$		
	1	t t t	V	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVI		Z $\overline{C}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVII		N $\overline{C}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVIII		H R Y J $\overline{M}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Remove the matrix assembly from the test jack.

100. Matrix Card Assembly 548130

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, T, U, W, X, Y, Z, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks $\overline{D}$ and DC voltages −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548130 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F T U Y		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
II		S W $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		R S W		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		R S $\overline{M}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		S $\overline{M}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VI		S Z $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		H T $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		$\overline{B}$ $\overline{H}$ $\overline{K}$		
	1	t t t	$\overline{D}$	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		R $\overline{K}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
X		H X $\overline{F}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		H J $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		K L		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIII		M N P $\overline{P}$		
	1	t t t t	V	0
	5	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XIV		P J $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XV		J L		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

101. Matrix Card Assembly 548132

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, T, U, V, W, X, Y, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{Y}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548132 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		$\overline{A}$ $\overline{F}$ J		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		S $\overline{F}$ $\overline{H}$ $\overline{M}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		R S $\overline{C}$ $\overline{F}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		H $\overline{C}$ $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VI		T $\overline{B}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		K M W $\overline{K}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		T $\overline{C}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		F R U Y		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		$\overline{F}$ $\overline{R}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XI		P $\overline{N}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		F N U Y		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XIII		T V $\overline{L}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XIV		F L X Y $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XV		F J L Y $\overline{T}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XVI		H $\overline{F}$ $\overline{M}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

102. Matrix Card Assembly 548134

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, F, H, J, K, L, M, N, P, S, T, U, X, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548134 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K P $\overline{A}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
II		J K L N P $\overline{B}$		
	1	t t t t t t	D	0
	2	f t t t t t	D	−6
	3	t f t t t t	D	−6
	4	t t f t t t	D	−6
	5	t t t f t t	D	−6
	6	t t t t f t	D	−6
	7	t t t t t f	D	−6
III		H K M P		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IV		F U X Z		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		F T X Z		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VI		F T Z $\overline{J}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		F S T X Z $\overline{F}$ $\overline{M}$		
	1	t t t t t t t	$\overline{U}$	0
	2	f t t t t t t	$\overline{U}$	−6
	3	t f t t t t t	$\overline{U}$	−6
	4	t t f t t t t	$\overline{U}$	−6
	5	t t t f t t t	$\overline{U}$	−6
	6	t t t t f t t	$\overline{U}$	−6
	7	t t t t t f t	$\overline{U}$	−6
	8	t t t t t t f	$\overline{U}$	−6
VIII		F U X Z		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IX		$\overline{P}$ $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		$\overline{N}$ $\overline{S}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XI		B		
	1	t	E	0
	2	f	E	−6
XII		$\overline{E}$ $\overline{H}$ $\overline{K}$ $\overline{L}$ $\overline{R}$		
	1	t t t t t	$\overline{T}$	0
	2	f t t t t	$\overline{T}$	−6
	3	t f t t t	$\overline{T}$	−6
	4	t t f t t	$\overline{T}$	−6
	5	t t t f t	$\overline{T}$	−6
	6	t t t t f	$\overline{T}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

103. Matrix Card Assembly 548136

Note. The schematic diagram is in TM 11–5840–272–30/20.

a. Set TRUE-FALSE switches D, E, J, L, N, S, T, U, W, X, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548136 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		T Y Z $\overline{P}$ T $\overline{U}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
II		D W Z J		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		U Z J $\overline{M}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		T Z $\overline{M}$ T $\overline{V}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		N $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		$\overline{C}$		
	1	t	V	0
	2	f	V	−6
VII		$\overline{F}$ $\overline{M}$ $\overline{R}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VIII		$\overline{F}$ $\overline{M}$ $\overline{N}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IX		Y $\overline{F}$ $\overline{L}$ $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
X		Y $\overline{F}$ $\overline{L}$ $\overline{N}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XI		E J		
	1	t t	F	0
	2	f t	F	−6
	3	t f	F	−6
XII		L S $\overline{A}$ $\overline{B}$ $\overline{E}$		
	1	t t t t t	F	0
	2	f t t t t	F	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t t	F	−6
	4	t t f t t	F	−6
	5	t t t f t	F	−6
	6	t t t t f	F	−6
XIII		$\overline{C}$		
	1	t	F	0
	2	f	F	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

104. Matrix Card Assembly 548138

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, M, N, P, R, S, T, U, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548138 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J M N S $\overline{E}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
II		N S $\overline{B}$ $\overline{E}$ $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
III		H P T Z $\overline{J}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
IV		H P T Z $\overline{T}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
V		E T		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		R T		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		$\overline{H}$ $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		E U X Y $\overline{F}$ $\overline{H}$ $\overline{N}$ $\overline{R}$		
	1	t t t t t t t t	$\overline{V}$	0
	2	f t t t t t t t	$\overline{V}$	−6
	3	t f t t t t t t	$\overline{V}$	−6
	4	t t f t t t t t	$\overline{V}$	−6
	5	t t t f t t t t	$\overline{V}$	−6
	6	t t t t f t t t	$\overline{V}$	−6
	7	t t t t t f t t	$\overline{V}$	−6
	8	t t t t t t f t	$\overline{V}$	−6
	9	t t t t t t t f	$\overline{V}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks F and $\overline{S}$.

j. Remove the matrix assembly from the test jack.

105. Matrix Card Assembly 548140

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches H, J, K, N, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548140 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
I		W	$\overline{K}$							
	1	t	t						C	0
	2	f	t						C	−6
	3	t	f						C	−6
II		H	J	W	$\overline{B}$					
	1	t	t	t	t				C	0
	2	f	t	t	t				C	−6
	3	t	f	t	t				C	−6
	4	t	t	f	t				C	−6
	5	t	t	t	f				C	−6
III		J	S	$\overline{F}$	$\overline{M}$	$\overline{U}$				
	1	t	t	t	t	t			C	0
	2	f	t	t	t	t			C	−6
	3	t	f	t	t	t			C	−6
	4	t	t	f	t	t			C	−6
	5	t	t	t	f	t			C	−6
	6	t	t	t	t	f			C	−6
IV		J	S	X	$\overline{F}$	$\overline{L}$	$\overline{U}$			
	1	t	t	t	t	t	t		C	0
	2	f	t	t	t	t	t		C	−6
	3	t	f	t	t	t	t		C	−6
	4	t	t	f	t	t	t		C	−6
	5	t	t	t	f	t	t		C	−6
	6	t	t	t	t	f	t		C	−6
	7	t	t	t	t	t	f		C	−6
V		T								
	1	t							V	0
	2	f							V	−6
VI		J	$\overline{F}$	$\overline{M}$						
	1	t	t	t					W	0
	2	f	t	t					W	−6
	3	t	f	t					W	−6
	4	t	t	f					W	−6
VII		P	Z	$\overline{A}$	$\overline{E}$	J	$\overline{K}$			
	1	t	t	t	t	t	t		W	0
	2	f	t	t	t	t	t		W	−6
	3	t	f	t	t	t	t		W	−6
	4	t	t	f	t	t	t		W	−6
	5	t	t	t	f	t	t		W	−6
	6	t	t	t	t	f	t		W	−6
	7	t	t	t	t	t	f		W	−6
VIII		K	P	Z	$\overline{E}$	$\overline{K}$	$\overline{T}$			
	1	t	t	t	t	t	t		W	0
	2	f	t	t	t	t	t		W	−6
	3	t	f	t	t	t	t		W	−6
	4	t	t	f	t	t	t		W	−6
	5	t	t	t	f	t	t		W	−6
	6	t	t	t	t	f	t		W	−6
	7	t	t	t	t	t	f		W	−6
IX		H	P	U	Y	$\overline{K}$	$\overline{P}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	W	0
	2	f	t	t	t	t	t	t	W	−6
	3	t	f	t	t	t	t	t	W	−6
	4	t	t	f	t	t	t	t	W	−6
	5	t	t	t	f	t	t	t	W	−6
	6	t	t	t	t	f	t	t	W	−6
	7	t	t	t	t	t	f	t	W	−6
	8	t	t	t	t	t	t	f	W	−6
X		K	N	R						
	1	t	t	t					W	0
	2	f	t	t					W	−6
	3	t	f	t					W	−6
	4	t	t	f					W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		K N $\overline{M}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack S and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

106. Matrix Card Assembly 548142

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches H, J, K, N, R, S, T, $\overline{A}$, $\overline{F}$, $\overline{H}$, J, $\overline{N}$, $\overline{P}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548142 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{F}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
II		$\overline{N}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
III		T $\overline{N}$		
	1	t t	E	0
	2	f t	E	−6
	3	t f	E	−6
IV		N $\overline{P}$ $\overline{A}$		
	1	t t t	E33[a]	0
	2	f t t	E33[a]	−6
	3	t f t	E33[a]	−6
	4	t t f	E33[a]	−6
V		H $\overline{N}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
VI		H $\overline{H}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VII		H $\overline{N}$ $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		H S $\overline{N}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		H J $\overline{N}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		H J J $\overline{N}$ $\overline{T}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
XI		H J $\overline{N}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches						Test point	Output voltage
	3	t	f	t	t	t		$\overline{C}$	−6
	4	t	t	f	t	t		$\overline{C}$	−6
	5	t	t	t	f	t		$\overline{C}$	−6
	6	t	t	t	t	f		$\overline{C}$	−6
XII		H	J	R	$\overline{N}$	$\overline{S}$	$\overline{T}$		
	1	t	t	t	t	t	t	D	0
	2	f	t	t	t	t	t	D	−6
	3	t	f	t	t	t	t	D	−6
	4	t	t	f	t	t	t	D	−6
	5	t	t	t	f	t	t	D	−6
	6	t	t	t	t	f	t	D	−6
	7	t	t	t	t	t	f	D	−6
XIII		H	J	K	$\overline{N}$	$\overline{S}$	$\overline{T}$		
	1	t	t	t	t	t	t	W	0
	2	f	t	t	t	t	t	W	−6
	3	t	f	t	t	t	t	W	−6
	4	t	t	f	t	t	t	W	−6
	5	t	t	t	f	t	t	W	−6
	6	t	t	t	t	f	t	W	−6
	7	t	t	t	t	t	f	W	−6

[a] Check at E33 on card assembly.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Set the AC VAR FREQUENCY switch to 1 KC.

i. Press the REF PULSE switch on.

j. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

k. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

l. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

m. Connect a jumper lead from E33 on card assembly to GRD.

n. Connect LOAD 1 between jacks $\overline{M}$ and SIGNALS REF PULSE with jumper leads, and set the LOAD 1 selector switch to position 8.

o. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack $\overline{M}$ is 20 to 40 μsec.

p. Remove the jumper leads.

q. Remove the matrix assembly from the test jack.

r. Return all TRUE-FALSE switches to neutral positions.

107. Matrix Card Assembly 548144

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches F, H, M, P, R, Z, $\overline{B}$, $\overline{H}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548144 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches		Test point	Output voltage
I		$\overline{B}$			
	1	t		$\overline{U}$	0
	2	f		$\overline{U}$	−6
II		F			
	1	t		$\overline{E}$	0
	2	f		$\overline{E}$	−6
III		P	$\overline{S}$		
	1	t	t	E	0
	2	f	t	E	−6
	3	t	f	E	−6
IV		F			
	1	t		U	0
	2	f		U	−6
V		F			
	1	t		$\overline{V}$	0
	2	f		$\overline{V}$	−6
VI		Z	$\overline{P}$		
	1	t	t	$\overline{C}$	0
	2	f	t	$\overline{C}$	−6
	3	t	f	$\overline{C}$	−6
VII		H			
	1	t		$\overline{C}$	0
	2	f		$\overline{C}$	−6
VIII		Z	$\overline{P}$		
	1	t	t	C	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t	C	−6
	3	t f	C	−6
IX		F Z		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		H Z		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		F $\overline{H}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XII		F $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		F R $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XIV		F M $\overline{R}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

108. Matrix Card Assembly 548146

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches H, J, K, L, M, N, P, R, S, X, Y, F, H, J, L, M, N, P, R, S, and T to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548146 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H J K L $\overline{F}$ $\overline{P}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t t	$\overline{W}$	0
	2	f t t t t t t t	$\overline{W}$	−6
	3	t f t t t t t t	$\overline{W}$	−6
	4	t t f t t t t t	$\overline{W}$	−6
	5	t t t f t t t t	$\overline{W}$	−6
	6	t t t t f t t t	$\overline{W}$	−6
	7	t t t t t f t t	$\overline{W}$	−6
	8	t t t t t t f t	$\overline{W}$	−6
	9	t t t t t t t f	$\overline{W}$	−6
II		$\overline{M}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		X Y $\overline{M}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		R $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		P		
	1	t	T	0
	2	f	T	−6
VI		R J $\overline{M}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VII		R $\overline{L}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		N $\overline{M}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		S $\overline{R}$		
	1	t t	F	0
	2	f t	F	−6
	3	t f	F	−6
X		M $\overline{R}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
XI		M $\overline{H}$ $\overline{R}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
XII		M $\overline{N}$ $\overline{R}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
XIII		S $\overline{N}$ $\overline{R}$		
	1	t t t	E	0
	2	f t t	E	−6
	3	t f t	E	−6
	4	t t f	E	−6
XIV		R $\overline{L}$ $\overline{M}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

109. Matrix Card Assembly 548148

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, M, P, $\overline{E}$, $\overline{H}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548148 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H J K $\overline{E}$ $\overline{N}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t	$\overline{V}$	0
	2	f t t t t t t	$\overline{V}$	−6
	3	t f t t t t t	$\overline{V}$	−6
	4	t t f t t t t	$\overline{V}$	−6
	5	t t t f t t t	$\overline{V}$	−6
	6	t t t t f t t	$\overline{V}$	−6
	7	t t t t t f t	$\overline{V}$	−6
	8	t t t t t t f	$\overline{V}$	−6
II		H J K $\overline{N}$ $\overline{P}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
III		F M $\overline{H}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IV		$\overline{R}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches								Test point	Output voltage
V		H	J	K	P	$\overline{N}$	$\overline{P}$	$\overline{S}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	t	C	−6
	6	t	t	t	t	f	t	t	t	C	−6
	7	t	t	t	t	t	f	t	t	C	−6
	8	t	t	t	t	t	t	f	t	C	−6
	9	t	t	t	t	t	t	t	f	C	−6
VI		H	J	K	L	$\overline{N}$	$\overline{P}$	$\overline{S}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	t	V	0
	2	f	t	t	t	t	t	t	t	V	−6
	3	t	f	t	t	t	t	t	t	V	−6
	4	t	t	f	t	t	t	t	t	V	−6
	5	t	t	t	f	t	t	t	t	V	−6
	6	t	t	t	t	f	t	t	t	V	−6
	7	t	t	t	t	t	f	t	t	V	−6
	8	t	t	t	t	t	t	f	t	V	−6
	9	t	t	t	t	t	t	t	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

110. Matrix Card Assembly 548151

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, R, S, T, X, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548151 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
I		H	J	K	R	X	$\overline{P}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	C	−6
	6	t	t	t	t	f	t	t	C	−6
	7	t	t	t	t	t	f	t	C	−6
	8	t	t	t	t	t	t	f	C	−6
II		K	S	T	X	$\overline{F}$	J	$\overline{K}$		
	1	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	C	−6
	6	t	t	t	t	f	t	t	C	−6
	7	t	t	t	t	t	f	t	C	−6
	8	t	t	t	t	t	t	f	C	−6
III		F	H	K	X	$\overline{F}$	$\overline{P}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	C	−6
	6	t	t	t	t	f	t	t	C	−6
	7	t	t	t	t	t	f	t	C	−6
	8	t	t	t	t	t	t	f	C	−6
IV		H	K	R	X	$\overline{P}$	$\overline{R}$			
	1	t	t	t	t	t	t		C	0
	2	f	t	t	t	t	t		C	−6
	3	t	f	t	t	t	t		C	−6
	4	t	t	f	t	t	t		C	−6
	5	t	t	t	f	t	t		C	−6
	6	t	t	t	t	f	t		C	−6
	7	t	t	t	t	t	f		C	−6
V		H	K	X	$\overline{H}$	$\overline{R}$	$\overline{T}$			
	1	t	t	t	t	t	t		C	0
	2	f	t	t	t	t	t		C	−6
	3	t	f	t	t	t	t		C	−6
	4	t	t	f	t	t	t		C	−6
	5	t	t	t	f	t	t		C	−6
	6	t	t	t	t	f	t		C	−6
	7	t	t	t	t	t	f		C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		H K R X $\overline{P}$ $\overline{S}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
VII		J K X $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VIII		E		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

111. Matrix Card Assembly 548153

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, L, R, $\overline{F}$, H, $\overline{S}$, T, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548153 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L		
	1	t	C, $\overline{V}$, $\overline{W}$	0
	2	f	C, $\overline{V}$, $\overline{W}$	−6
II		E F $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
III		E $\overline{U}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IV		E H R $\overline{F}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		E H R $\overline{S}$ $\overline{T}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VI		E F $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		E H $\overline{H}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VIII		E H $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		E R $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		E $\overline{S}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{P}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

112. Matrix Card Assembly 548155

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, H, J, L, P, R, S, $\overline{F}$, $\overline{H}$, J, $\overline{P}$, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548155 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H J P S $\overline{P}$ $\overline{T}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
II		L		
	1	t	V, $\overline{C}$	0
	2	f	V, $\overline{C}$	−6
III		E $\overline{F}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IV		E $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		H J P $\overline{J}$ $\overline{P}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
VI		E $\overline{H}$ $\overline{J}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VII		E R $\overline{J}$ $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VIII		H J P $\overline{P}$ $\overline{T}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		E $\overline{F}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		E $\overline{H}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

113. Matrix Card Assembly 548157

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, L, P, R, T, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548157 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H P T $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		E R T $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		E R T $\overline{H}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		E F T $\overline{F}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		L		
	1	t	V, $\overline{C}$	0
	2	f	V, $\overline{C}$	−6
VI		H J P $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		E J $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		E J $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		H P $\overline{K}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
X		H P $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XI		E F $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		E $\overline{R}$ $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

114. Matrix Card Assembly 548159

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, H, J, L, N, R, S, T, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548159 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N $\overline{P}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
II		L $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		J Y		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IV		T X		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		$\overline{B}$ $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		Z $\overline{J}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		H $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		S $\overline{L}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IX		$\overline{R}$		
	1	t	E	0
	2	f	E	−6
X		$\overline{F}$		
	1	t	U	0
	2	f	U	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		F		
	1	t	W	0
	2	f	W	−6
XII		R		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIII		$\overline{S}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
XIV		$\overline{H}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XV		$\overline{A}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks F, R, $\overline{A}$, $\overline{F}$, $\overline{H}$, $\overline{R}$, and $\overline{S}$.

j. Remove the matrix assembly from the test jack.

115. Matrix Card Assembly 548161

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548161 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E K $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		F S T Y $\overline{H}$ $\overline{K}$ $\overline{L}$ $\overline{R}$ $\overline{T}$		
	1	t t t t t t t t t	V	0
	2	f t t t t t t t t	V	−6
	3	t f t t t t t t t	V	−6
	4	t t f t t t t t t	V	−6
	5	t t t f t t t t t	V	−6
	6	t t t t f t t t t	V	−6
	7	t t t t t f t t t	V	−6
	8	t t t t t t f t t	V	−6
	9	t t t t t t t f t	V	−6
	10	t t t t t t t t f	V	−6
III		F S T Y $\overline{H}$ $\overline{M}$ $\overline{R}$ $\overline{T}$		
	1	t t t t t t t t	V	0
	2	f t t t t t t t	V	−6
	3	t f t t t t t t	V	−6
	4	t t f t t t t t	V	−6
	5	t t t f t t t t	V	−6
	6	t t t t f t t t	V	−6
	7	t t t t t f t t	V	−6
	8	t t t t t t f t	V	−6
	9	t t t t t t t f	V	−6
IV		U $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		P U Z		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		E K $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		J N S $\overline{J}$ $\overline{L}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t t t	$\overline{D}$	0

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
	2	f	t	t	t	t	t	t	$\overline{D}$	−6
	3	t	f	t	t	t	t	t	$\overline{D}$	−6
	4	t	t	f	t	t	t	t	$\overline{D}$	−6
	5	t	t	t	f	t	t	t	$\overline{D}$	−6
	6	t	t	t	t	f	t	t	$\overline{D}$	−6
	7	t	t	t	t	t	f	t	$\overline{D}$	−6
	8	t	t	t	t	t	t	f	$\overline{D}$	−6
VIII		L	R	$\overline{F}$	$\overline{N}$	$\overline{S}$				
	1	t	t	t	t	t			$\overline{D}$	0
	2	f	t	t	t	t			$\overline{D}$	−6
	3	t	f	t	t	t			$\overline{D}$	−6
	4	t	t	f	t	t			$\overline{D}$	−6
	5	t	t	t	f	t			$\overline{D}$	−6
	6	t	t	t	t	f			$\overline{D}$	−6
IX		$\overline{E}$	$\overline{H}$							
	1	t	t						$\overline{D}$	0
	2	f	t						$\overline{D}$	−6
	3	t	f						$\overline{D}$	−6
X		P	$\overline{A}$	$\overline{B}$	$\overline{E}$					
	1	t	t	t	t				$\overline{D}$	0
	2	f	t	t	t				$\overline{D}$	−6
	3	t	f	t	t				$\overline{D}$	−6
	4	t	t	f	t				$\overline{D}$	−6
	5	t	t	t	f				$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and jacks H, U, and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

116. Matrix Card Assembly 548163

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, N, P, R, S, T, U, V, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548163 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches														Test point	Output voltage
I		E	F	H	J	K	N	W	Y	$\overline{A}$	$\overline{N}$	$\overline{P}$	$\overline{R}$	$\overline{S}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	t	t	t	t	t	t	t	∇	0
	2	f	t	t	t	t	t	t	t	t	t	t	t	t	t	∇	−6
	3	t	f	t	t	t	t	t	t	t	t	t	t	t	t	∇	−6
	4	t	t	f	t	t	t	t	t	t	t	t	t	t	t	∇	−6
	5	t	t	t	f	t	t	t	t	t	t	t	t	t	t	∇	−6
	6	t	t	t	t	f	t	t	t	t	t	t	t	t	t	∇	−6
	7	t	t	t	t	t	f	t	t	t	t	t	t	t	t	∇	−6
	8	t	t	t	t	t	t	f	t	t	t	t	t	t	t	∇	−6
	9	t	t	t	t	t	t	t	f	t	t	t	t	t	t	∇	−6
	10	t	t	t	t	t	t	t	t	f	t	t	t	t	t	∇	−6
	11	t	t	t	t	t	t	t	t	t	f	t	t	t	t	∇	−6
	12	t	t	t	t	t	t	t	t	t	t	f	t	t	t	∇	−6
	13	t	t	t	t	t	t	t	t	t	t	t	f	t	t	∇	−6
	14	t	t	t	t	t	t	t	t	t	t	t	t	f	t	∇	−6
	15	t	t	t	t	t	t	t	t	t	t	t	t	t	f	∇	−6

Test No.	Step No.	TRUE-FALSE switches														Test point	Output voltage
II		P	R	S	T	U	V	X	Z	$\overline{B}$	$\overline{E}$	$\overline{F}$	$\overline{H}$	J	$\overline{K}$		
	1	t	t	t	t	t	t	t	t	t	t	t	t	t	t	$\overline{V}$	0
	2	f	t	t	t	t	t	t	t	t	t	t	t	t	t	$\overline{V}$	−6
	3	t	f	t	t	t	t	t	t	t	t	t	t	t	t	$\overline{V}$	−6
	4	t	t	f	t	t	t	t	t	t	t	t	t	t	t	$\overline{V}$	−6
	5	t	t	t	f	t	t	t	t	t	t	t	t	t	t	$\overline{V}$	−6
	6	t	t	t	t	f	t	t	t	t	t	t	t	t	t	$\overline{V}$	−6
	7	t	t	t	t	t	f	t	t	t	t	t	t	t	t	$\overline{V}$	−6
	8	t	t	t	t	t	t	f	t	t	t	t	t	t	t	$\overline{V}$	−6
	9	t	t	t	t	t	t	t	f	t	t	t	t	t	t	$\overline{V}$	−6
	10	t	t	t	t	t	t	t	t	f	t	t	t	t	t	$\overline{V}$	−6
	11	t	t	t	t	t	t	t	t	t	f	t	t	t	t	$\overline{V}$	−6
	12	t	t	t	t	t	t	t	t	t	t	f	t	t	t	$\overline{V}$	−6
	13	t	t	t	t	t	t	t	t	t	t	t	f	t	t	$\overline{V}$	−6
	14	t	t	t	t	t	t	t	t	t	t	t	t	f	t	$\overline{V}$	−6
	15	t	t	t	t	t	t	t	t	t	t	t	t	t	f	$\overline{V}$	−6
III		F[a]															
	1	t														$\overline{V}$	0
	2	f														$\overline{V}$	−6
IV		S[a]															
	1	t														$\overline{V}$	0
	2	f														$\overline{V}$	−6
V		$\overline{S}$[a]															
	1	t														$\overline{V}$	0
	2	f														$\overline{V}$	−6
VI		$\overline{U}$															
	1	t														$\overline{C}$	0
	2	f														$\overline{C}$	−6

[a] Set TRUE-FALSE switches E, H, J, K, N, R, W, Y, $\overline{A}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{P}$, and $\overline{R}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

117. Matrix Card Assembly 548165

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, P, R, S, T, U, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548165 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		E		
	1	t	V, X	0
	2	f	V, X	−6
I		J P		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		T $\overline{E}$ $\overline{F}$ J		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
V		F J $\overline{P}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
V		H K R J $\overline{P}$ $\overline{R}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
VI		$\overline{T}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VII		E U		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		S $\overline{H}$ $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		E K		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		E K $\overline{E}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
XI		E T		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XII		E K $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIII		F H $\overline{R}$ $\overline{T}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XIV		R $\overline{H}$ $\overline{R}$ $\overline{T}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{R}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

118. Matrix Card Assembly 548167

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, R, S, T, $\overline{F}$, $\overline{H}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548167 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E K T $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		F H $\overline{R}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		R $\overline{H}$ $\overline{R}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		E J K $\overline{R}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		H $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		E J K $\overline{F}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VII		H $\overline{H}$ $\overline{T}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VIII		E J K $\overline{P}$ $\overline{R}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
IX		$\overline{T}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
X		S $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XI		H $\overline{T}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks H, J, S, T, F, P, and $\overline{S}$.

j. Remove the matrix assembly from the test jack.

119. Matrix Card Assembly 548169

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, M, N, P, R, T, U, X, Y, Z, $\overline{A}$, $\overline{H}$, J, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548169 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H R $\overline{S}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		F H $\overline{S}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		Z $\overline{V}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		J		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
V		H R $\overline{H}$ $\overline{P}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VI		M P		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		U $\overline{A}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		H K R $\overline{H}$ $\overline{P}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
IX		N X Y		
	1	t t t	D, $\overline{C}$	0
	2	f t t	D, $\overline{C}$	−6
	3	t f t	D, $\overline{C}$	−6
	4	t t f	D, $\overline{C}$	−6
X		E M T		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XI		E M T $\overline{J}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
XII		E M $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks F, P, and J.

j. Remove the matrix assembly from the test jack.

120. Matrix Card Assembly 548171

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, M, N, X, Y, $\overline{A}$, $\overline{F}$, $\overline{K}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548171 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F $\overline{S}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
II		F $\overline{F}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
III		F K $\overline{A}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IV		F J $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		E M $\overline{K}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VI		E M $\overline{T}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		N X Y		
	1	t t t	$\overline{D}$, V	0
	2	f t t	$\overline{D}$, V	−6
	3	t f t	$\overline{D}$, V	−6
	4	t t f	$\overline{D}$, V	−6
VIII		E M $\overline{T}$ $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		E H M		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks H, $\overline{K}$, and $\overline{U}$.

j. Remove the matrix assembly from the test jack.

121. Matrix Card Assembly 548173

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F H, J, K, N, P, R, S, T, U, Y, Z, $\overline{A}$, B, $\overline{E}$, F, H, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548173 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		U R S T Z F H		
	1	t t t t t t t	C	0
	2	f t t t t t t	C	−6
	3	t f t t t t t	C	−6
	4	t t f t t t t	C	−6
	5	t t t f t t t	C	−6
	6	t t t t f t t	C	−6
	7	t t t t t f t	C	−6
	8	t t t t t t f	C	−6
I		U R S T Y F H		
	1	t t t t t t t	C	0
	2	f t t t t t t	C	−6
	3	t f t t t t t	C	−6
	4	t t f t t t t	C	−6
	5	t t t f t t t	C	−6
	6	t t t t f t t	C	−6
	7	t t t t t f t	C	−6
	8	t t t t t t f	C	−6
II		K		
	1	t	W	0
	2	f	W	−6
V		F $\overline{A}$ $\overline{S}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
		F H $\overline{A}$ $\overline{B}$ $\overline{H}$ $\overline{L}$		
	1	t t t t t t	W	0
	2	f t t t t t	W	−6
	3	t f t t t t	W	−6
	4	t t f t t t	W	−6
	5	t t t f t t	W	−6
	6	t t t t f t	W	−6
	7	t t t t t f	W	−6
I		$\overline{T}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
II		$\overline{H}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		R		
	1	t	D	0
	2	f	D	−6
IX		E		
	1	t	V	0
	2	f	V	−6
X		Z $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		J R $\overline{M}$ $\overline{P}$ $\overline{R}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XII		$\overline{E}$ $\overline{N}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XIII		P $\overline{N}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Set the AC VAR FREQUENCY switch to 1 KC.

i. Press the REF PULSE switch on.

j. Synchronize the oscilloscope for a negative signal to the SYNC SIGNAL connector.

k. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

l. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

m. Set TRUE-FALSE switch N to TRUE.

n. Connect a load between jack L and SIGNALS

REF PULSE with jumper leads, and set the LOAD selector switch to position 8.

o. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack L is 30 to 50 μsec.

p. Remove the matrix assembly from the test jack.

q. Return all TRUE-FALSE switches to neutral positions.

122. Matrix Card Assembly 548175

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, Z, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548175 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F Z $\overline{K}$ $\overline{B}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
II		F Z $\overline{B}$ $\overline{K}$		
	1	t t t t	$\overline{V}$	0
	2	t t f t	$\overline{V}$	−6
III		F Z $\overline{K}$ $\overline{M}$		
	1	t t t t	$\overline{V}$	0
	2	t t t f	$\overline{V}$	−6
IV		F Z $\overline{F}$ $\overline{K}$		
	1	t t t t	$\overline{V}$	0
	2	t t f t	$\overline{V}$	−6
V		$\overline{P}$ $\overline{U}$		
	1	t t	D, $\overline{C}$	0
	2	f t	D, $\overline{C}$	−6
	3	t f	D, $\overline{C}$	−6
VI		$\overline{E}$		
	1	t	W	0
	2	f	W	−6
VII		E $\overline{S}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VIII		E $\overline{J}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		E $\overline{T}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		E $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

123. Matrix Card Assembly 548177

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, F, J, K, N, P, R, S, T, U, Y, $\overline{A}$, J, $\overline{M}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548177 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		$\overline{U}$		
	1	t	V	0
	2	f	V	−6
I		E Y		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
II		P $\overline{J}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		$\overline{A}$		
	1	t	$\overline{D}$, W	0
	2	f	$\overline{D}$, W	−6
		R		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
I		F N R S T $\overline{M}$		
	1	t t t t t t	D	0
	2	f t t t t t	D	−6
	3	t f t t t t	D	−6
	4	t t f t t t	D	−6
	5	t t t f t t	D	−6
	6	t t t t f t	D	−6
	7	t t t t t f	D	−6
II		K N R S T		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT witches off.

h. Set the AC VAR FREQUENCY switch to 1 C.

i. Press the REF PULSE switch on.

j. Synchronize the oscilloscope for a negative gnal to the SYNC SIGNAL connector.

k. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

l. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

m. Set TRUE-FALSE switches J and $\overline{R}$ to TRUE.

n. Connect a load between jack L and SIGNALS REF PULSE with jumper leads, and set the LOAD selector switch to position 8.

o. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack L is 16 to 24 μsec.

p. Remove the jumper from the jack L, and connect to jack $\overline{N}$.

q. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack $\overline{N}$ is 16 to 24 μsec.

r. Return all TRUE-FALSE switches to neutral positions.

s. Measure 10,000 ohms between jacks U and $\overline{Y}$.

t. Remove the matrix assembly from the test jack.

124. Matrix Card Assembly 548179

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, M, N, P, R, S, T, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{L}$, $\overline{M}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548179 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{M}$		
	1	t	U	0
	2	f	U	−6
II		$\overline{F}$		
	1	t	U	0
	2	f	U	−6
III		S		
	1	t	U, W	0
	2	f	U, W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IV		P		
	1	t	U	0
	2	f	U	−6
V		F		
	1	t	U	0
	2	f	U	−6
VI		H N		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
VII		R		
	1	t	W	0
	2	f	W	−6
VIII		$\overline{H}$		
	1	t	$\overline{C}$, W	0
	2	f	$\overline{C}$, W	−6
IX		J		
	1	t	W	0
	2	f	W	−6
X		$\overline{S}$		
	1	t	W	0
	2	f	W	−6
XI		T		
	1	t	W	0
	2	f	W	−6
XII		K		
	1	t	W	0
	2	f	W	−6
XIII		M		
	1	t	W	0
	2	f	W	−6
XIV		R		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XV		J		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XVI		$\overline{L}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XVII		$\overline{E}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks E and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

125. Matrix Card Assembly 548183

Note. The schematic diagram is in TM 11-5840-271-3 /20.

a. Set TRUE-FALSE switches E, F, H, J, N, P, R, S, T, U, V, W, X, Y, Z, $\overline{A}$, B, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548183 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{U}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches														Test point	Output voltage
II		E	F	H	J	N	V	X	Z	$\overline{B}$	$\overline{F}$	$\overline{P}$	$\overline{R}$	$\overline{S}$	$\overline{T}$		
	1	t	t	t	t	t	t	t	t	t	t	t	t	t	t	W	0
	2	f	t	t	t	t	t	t	t	t	t	t	t	t	t	W	−6
	3	t	f	t	t	t	t	t	t	t	t	t	t	t	t	W	−6
	4	t	t	f	t	t	t	t	t	t	t	t	t	t	t	W	−6
	5	t	t	t	f	t	t	t	t	t	t	t	t	t	t	W	−6
	6	t	t	t	t	f	t	t	t	t	t	t	t	t	t	W	−6
	7	t	t	t	t	t	f	t	t	t	t	t	t	t	t	W	−6
	8	t	t	t	t	t	t	f	t	t	t	t	t	t	t	W	−6
	9	t	t	t	t	t	t	t	f	t	t	t	t	t	t	W	−6
	10	t	t	t	t	t	t	t	t	f	t	t	t	t	t	W	−6
	11	t	t	t	t	t	t	t	t	t	f	t	t	t	t	W	−6
	12	t	t	t	t	t	t	t	t	t	t	f	t	t	t	W	−6
	13	t	t	t	t	t	t	t	t	t	t	t	f	t	t	W	−6
	14	t	t	t	t	t	t	t	t	t	t	t	t	f	t	W	−6
	15	t	t	t	t	t	t	t	t	t	t	t	t	t	f	W	−6
III		P	R	S	T	U	W	Y	$\overline{A}$	$\overline{C}$	$\overline{E}$	$\overline{H}$	J	$\overline{K}$	$\overline{L}$	$\overline{P}$	
	1	t	t	t	t	t	t	t	t	t	t	t	t	t	t	W	0
	2	f	t	t	t	t	t	t	t	t	t	t	t	t	t	W	−6
	3	t	f	t	t	t	t	t	t	t	t	t	t	t	t	W	−6
	4	t	t	f	t	t	t	t	t	t	t	t	t	t	t	W	−6
	5	t	t	t	f	t	t	t	t	t	t	t	t	t	t	W	−6
	6	t	t	t	t	f	t	t	t	t	t	t	t	t	t	W	−6
	7	t	t	t	t	t	f	t	t	t	t	t	t	t	t	W	−6
	8	t	t	t	t	t	t	f	t	t	t	t	t	t	t	W	−6
	9	t	t	t	t	t	t	t	f	t	t	t	t	t	t	W	−6
	10	t	t	t	t	t	t	t	t	f	t	t	t	t	t	W	−6
	11	t	t	t	t	t	t	t	t	t	f	t	t	t	t	W	−6
	12	t	t	t	t	t	t	t	t	t	t	f	t	t	t	W	−6
	13	t	t	t	t	t	t	t	t	t	t	t	f	t	t	W	−6
	14	t	t	t	t	t	t	t	t	t	t	t	t	f	t	W	−6
	15	t	t	t	t	t	t	t	t	t	t	t	t	t	f	W	−6
IV		J[a]															
	1	t														W	0
	2	f														W	−6
V		S[a]															
	1	t														W	0
	2	f														W	−6
VI		$\overline{P}$[a]															
	1	t														W	0
	2	f														W	−6

[a] Set TRUE-FALSE switches E, F, H, T, U, V, X, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{K}$, $\overline{R}$, and $\overline{S}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

126. Matrix Card Assembly 548185

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, P, R, S, T, U, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548185 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K		
	1	t	X	0
	2	f	X	−6
II		F $\overline{T}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
III		K		
	1	t	V	0
	2	f	V	−6
IV		R $\overline{F}$ $\overline{H}$ J		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
V		E H U $\overline{F}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
VI		J $\overline{F}$ $\overline{P}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VII		$\overline{T}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VIII		K P		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IX		S $\overline{E}$ $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
X		E $\overline{K}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XI		E K $\overline{J}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
XII		J $\overline{T}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XIII		H J $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		E K $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XV		U $\overline{E}$ $\overline{S}$ T		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off and return all TRUE-FALSE switches to neutral positions.

h. Measure 10,000 ohms between jacks $\overline{S}$ and $\overline{Y}$.

i. Set the AC VAR FREQUENCY switch to 1 KC.

j. Press the REF PULSE switch on.

k. Synchronize the oscilloscope for a negative signal and connect to the SYNC SIGNAL connector.

l. Set the REF PULSE AMPLITUDE switch to −, and adjust the REF PULSE AMPLITUDE control for a −6-volt output.

m. Set the REF PULSE DURATION switch to LONG, and adjust the REF PULSE DURATION control for a 500-μsec pulse width.

n. Set TRUE-FALSE switch N to TRUE.

o. Connect LOAD 1 between jack L and SIGNALS REF PULSE with jumper leads, and set the LOAD 1 selector switch to position 9.

p. Observe that the 0 to 85 percent risetime of the negative-going waveform at jack L is 40 to 60 μsec.

q. Remove the jumper leads.

r. Remove the matrix assembly from the test jack.

127. Matrix Card Assembly 548187

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, R, S, U, $\overline{E}$, $\overline{H}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548187 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E K R $\overline{S}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		H J $\overline{S}$ T		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		U $\overline{E}$ $\overline{S}$ T		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		E F K $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		H $\overline{E}$ $\overline{T}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VI		E F K $\overline{H}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		H $\overline{P}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		E F K $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
IX		$\overline{T}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
X		S $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XI		H $\overline{T}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and R, $\overline{Y}$ and H, $\overline{Y}$ and F, $\overline{Y}$ and $\overline{R}$, and $\overline{Y}$ and $\overline{E}$.

j. Remove the matrix assembly from the test jack.

128. Matrix Card Assembly 548189

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, K, T, U, Y, Z, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548189 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H U $\overline{P}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		H J $\overline{P}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		Y $\overline{F}$ $\overline{H}$ $\overline{K}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IV		Y $\overline{F}$ $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		Z $\overline{B}$		
	1	t t	$\overline{C}$, $\overline{D}$, D	0
	2	f t	$\overline{C}$, $\overline{D}$, D	−6
	3	t f	$\overline{C}$, $\overline{D}$, D	−6
VI		Y $\overline{F}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		T Y		
	1	t t	D	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t	D	−6
	3	t f	D	−6
VIII		K Y $\overline{H}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IX		Y $\overline{F}$ J $\overline{S}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and J, $\overline{Y}$ and $\overline{J}$, $\overline{Y}$ and K, $\overline{Y}$ and $\overline{K}$, $\overline{Y}$ and $\overline{R}$, $\overline{Y}$ and $\overline{S}$, $\overline{Y}$ and T, and $\overline{Y}$ and U.

j. Remove the matrix assembly from the test jack.

129. Matrix Card Assembly 548191

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, T, U, $\overline{E}$, $\overline{H}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548191 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K L		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		K T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		E K L		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IV		F K $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		P R S U $\overline{E}$ $\overline{H}$ $\overline{M}$		
	1	t t t t t t t	D	0
	2	f t t t t t t	D	−6
	3	t f t t t t t	D	−6
	4	t t f t t t t	D	−6
	5	t t t f t t t	D	−6
	6	t t t t f t t	D	−6
	7	t t t t t f t	D	−6
	8	t t t t t t f	D	−6
VI		$\overline{U}$		
	1	t	W	0
	2	f	W	−6
VII		H J N $\overline{E}$ $\overline{L}$ $\overline{N}$		
	1	t t t t t t	$\overline{V}$	0
	2	f t t t t t	$\overline{V}$	−6
	3	t f t t t t	$\overline{V}$	−6
	4	t t f t t t	$\overline{V}$	−6
	5	t t t f t t	$\overline{V}$	−6
	6	t t t t f t	$\overline{V}$	−6
	7	t t t t t f	$\overline{V}$	−6
VIII		J $\overline{L}$ $\overline{P}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		N $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
X		F N U $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks E and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

130. Matrix Card Assembly 548192

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, K, N, P, R, S, U, X, Y, Z, $\overline{B}$, $\overline{E}$, F, J, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548192 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R $\overline{U}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		F		
	1	t	C	0
	2	f	C	−6
III		H U $\overline{E}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		P S $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		E H U $\overline{E}$ $\overline{R}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		N Y $\overline{F}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VII		Y $\overline{F}$ $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		Z $\overline{B}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		$\overline{N}$		
	1	t	D, T	0
	2	f	D, T	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		J		
	1	t	L, W	0
	2	f	L, W	−6
XI		K		
	1	t	$\overline{A}$, $\overline{C}$, $\overline{V}$	0
	2	f	$\overline{A}$, $\overline{C}$, $\overline{V}$	−6
XII		X		
	1	t	H, $\overline{X}$	0
	2	f	H, $\overline{X}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

131. Matrix Card Assembly 548197

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, K, L, P, R, S, T, X, Y, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548197 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P $\overline{F}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
II		K L $\overline{B}$ $\overline{K}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
III		H K L $\overline{B}$ $\overline{K}$ $\overline{P}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
IV		K L $\overline{B}$ $\overline{K}$ $\overline{R}$ $\overline{T}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
V		K L S J $\overline{K}$ $\overline{N}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
VI		X $\overline{P}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		K L $\overline{E}$ $\overline{K}$ $\overline{N}$ $\overline{R}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		K R T $\overline{B}$ $\overline{K}$ $\overline{R}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
IX		F K T $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		F K L Y $\overline{B}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XI		F K L $\overline{H}$ $\overline{N}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

132. Matrix Card Assembly 548199

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, L, M, N, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548199 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F J P		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		E J U		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		P R U		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		E F R		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t	$\overline{C}$	−6
V		S $\overline{R}$ $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		$\overline{F}$ $\overline{R}$ $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		L $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		N $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IX		T $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
X		$\overline{E}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		H M $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		M $\overline{H}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		M Y $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		M J $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XV		W $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVI		X $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVII		$\overline{K}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVIII		Z $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIX		$\overline{A}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XX		$\overline{D}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

133. Matrix Card Assembly 548201

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, H, J, K, L, R, U, W, X, Y, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548201 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false).

Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K $\overline{B}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		K $\overline{H}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		E $\overline{J}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		$\overline{E}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		$\overline{L}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		E $\overline{A}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		$\overline{M}$ $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		E $\overline{C}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		E $\overline{D}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		E $\overline{F}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		E $\overline{N}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		E $\overline{P}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		L $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIV		R $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XV		U $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVI		W $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVII		X $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVIII		Y $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIX		H $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XX		J		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

134. Matrix Card Assembly 548205

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, R, S, T, U, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548205 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F J		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		R U		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		N		
	1	t	V	0
	2	f	V	−6
IV		$\overline{B}$ $\overline{N}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
V		E $\overline{L}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VI		$\overline{B}$ $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VII		E $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		$\overline{U}$		
	1	t	D	0
	2	f	D	−6
IX		$\overline{J}$		
	1	t	W	0
	2	f	W	−6
X		K N		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XI		E S		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XII		T $\overline{F}$		
	1	t t	$\overline{W}$	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XIII		H L		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XIV		H T $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XV		K $\overline{H}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XVI		$\overline{T}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{R}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

135. Matrix Card Assembly 548207

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, K, N, P, S, T, V, Y, Z, $\overline{B}$, $\overline{C}$, $\overline{E}$, H, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548207 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N S $\overline{C}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
II		V $\overline{E}$ $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
III		F Z $\overline{R}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IV		V $\overline{E}$ $\overline{K}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		F $\overline{B}$ $\overline{K}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VI		$\overline{P}$		
	1	t	U	0
	2	f	U	−6
VII		P S $\overline{C}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
VIII		Y $\overline{E}$ $\overline{R}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		F $\overline{B}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
X		V $\overline{E}$ $\overline{K}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
XI		F Z $\overline{K}$ $\overline{S}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
XII		$\overline{T}$		
	1	t	U	0
	2	f	U	−6
XIII		K S T $\overline{E}$ $\overline{H}$		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

136. Matrix Card Assembly 548208

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, J, K, L, N, P, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548208 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{H}$ $\overline{M}$ $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		P $\overline{L}$ $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
III		P $\overline{J}$ $\overline{M}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		$\overline{H}$ $\overline{J}$ $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		E $\overline{H}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		K L T		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		J K N P		
	1	t t t t	V	0
	2	f t t t	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		J L P U		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		N T U		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		E T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		X $\overline{A}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XII		X $\overline{B}$ $\overline{E}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XIII		X $\overline{E}$ $\overline{U}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XIV		Y		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XV		Z $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

137. Matrix Card Assembly 548209

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, J, K, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, J, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548209 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P $\overline{R}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		F $\overline{E}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
III		$\overline{K}$ $\overline{S}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		J $\overline{T}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
V		$\overline{P}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		E Y		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		$\overline{N}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
VIII		$\overline{P}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IX		M		
	1	t	H	0
	2	f	H	−6
X		J L U		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XI		K L T		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XII		Z $\overline{F}$		
	1	t t	$\overline{H}$	0
	2	f t	$\overline{H}$	−6
	3	t f	$\overline{H}$	−6
XIII		Z $\overline{U}$		
	1	t t	$\overline{L}$	0
	2	f t	$\overline{L}$	−6
	3	t f	$\overline{L}$	−6
XIV		R S $\overline{M}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XV		X $\overline{B}$ $\overline{M}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XVI		N T U		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVII		J K N		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVIII		Y		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

138. Matrix Card Assembly 548210

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, P, $\overline{E}$, J, $\overline{K}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548210 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		P		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
III		$\overline{T}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
IV		$\overline{K}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
V		P $\overline{R}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VI		P $\overline{E}$ $\overline{K}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		F $\overline{E}$ $\overline{J}$ $\overline{K}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VIII		F J $\overline{R}$ $\overline{T}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IX		F $\overline{K}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
X		F $\overline{E}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XI		P $\overline{E}$ J $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XII		P J $\overline{K}$ $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

139. Matrix Card Assembly 548211

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches H, J, K, L, N, R, S, T, U, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548211 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H $\overline{A}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		T $\overline{A}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
III		N S $\overline{N}$ $\overline{P}$ $\overline{U}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		L S $\overline{H}$ $\overline{N}$ $\overline{U}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		J $\overline{A}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		H $\overline{A}$		
	1	t t	E	0
	2	f t	E	−6
	3	t f	E	−6
VII		T $\overline{A}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6
VIII		J $\overline{A}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		R $\overline{A}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		K $\overline{M}$ $\overline{R}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
XI		U $\overline{E}$ $\overline{M}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
XII		Z J $\overline{K}$		
	1	t t t	$\overline{S}$	0
	2	f t t	$\overline{S}$	−6
	3	t f t	$\overline{S}$	−6
	4	t t f	$\overline{S}$	−6
XIII		K $\overline{E}$ $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIV		U $\overline{L}$ $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XV		Y		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

140. Matrix Card Assembly 548212

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, L, M, P, R, S, T, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548212 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L		
	1	t	C	0
	2	f	C	−6
II		$\overline{L}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
III		$\overline{M}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IV		P $\overline{F}$ $\overline{U}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		F $\overline{E}$ $\overline{U}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		$\overline{K}$ $\overline{S}$ $\overline{U}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VII		J $\overline{T}$ $\overline{U}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VIII		$\overline{N}$		
	1	t	W	0
	2	f	W	−6
IX		S Z $\overline{H}$ $\overline{N}$ $\overline{U}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
X		S Y $\overline{N}$ $\overline{P}$ $\overline{U}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
XI		M $\overline{A}$ $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		R T $\overline{A}$		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6
XIII		E $\overline{A}$ $\overline{R}$		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6
XIV		R $\overline{A}$ $\overline{R}$		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XV		E T $\overline{A}$		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

141. Matrix Card Assembly 548214

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, P, R, $\overline{A}$, $\overline{B}$, F, H, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548214 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{B}$ H		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
II		$\overline{B}$ $\overline{T}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
III		$\overline{B}$ T $\overline{U}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		$\overline{B}$ F $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		P $\overline{B}$ $\overline{T}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VI		J $\overline{A}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		H $\overline{B}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		H K R $\overline{B}$		
	1	t t t t	$\overline{X}$	0
	2	f t t t	$\overline{X}$	−6
	3	t f t t	$\overline{X}$	−6
	4	t t f t	$\overline{X}$	−6
	5	t t t f	$\overline{X}$	−6
IX		F $\overline{B}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		H L R $\overline{B}$		
	1	t t t t	$\overline{E}$	0
	2	f t t t	$\overline{E}$	−6
	3	t f t t	$\overline{E}$	−6
	4	t t f t	$\overline{E}$	−6
	5	t t t f	$\overline{E}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

142. Matrix Card Assembly 548215

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches C, D, E, F, K, N, P, T, V, W, Z, $\overline{B}$, $\overline{C}$, $\overline{F}$, J, $\overline{L}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548215 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{F}$ $\overline{L}$ $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		Z $\overline{B}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		D $\overline{F}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		N J $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		V J $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VI		W $\overline{C}$ J		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		E J		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		K $\overline{V}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		K $\overline{W}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		C D K $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		P $\overline{V}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		P $\overline{W}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		F P $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIV		T $\overline{P}$ $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XV		T $\overline{L}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

143. Matrix Card Assembly 548217

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, L, N, P, S, U, W, Y, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks $\overline{D}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548217 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{U}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
II		F P $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		F U		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		J $\overline{E}$ $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		J $\overline{L}$ $\overline{M}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VI		E J		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		J $\overline{A}$ $\overline{B}$ $\overline{C}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		N $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		H L N W Y $\overline{N}$		
	1	t t t t t t	$\overline{D}$	0
	2	f t t t t t	$\overline{D}$	−6
	3	t f t t t t	$\overline{D}$	−6
	4	t t f t t t	$\overline{D}$	−6
	5	t t t f t t	$\overline{D}$	−6
	6	t t t t f t	$\overline{D}$	−6
	7	t t t t t f	$\overline{D}$	−6
X		S $\overline{P}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		$\overline{F}$ $\overline{P}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

144. Matrix Card Assembly 548219

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, R, S, T, U, X, Y, Z, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548219 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J L R X $\overline{B}$ $\overline{D}$ $\overline{M}$		
	1	t t t t t t t	C	0
	2	f t t t t t t	C	−6
	3	t f t t t t t	C	−6
	4	t t f t t t t	C	−6
	5	t t t f t t t	C	−6
	6	t t t t f t t	C	−6
	7	t t t t t f t	C	−6
	8	t t t t t t f	C	−6
II		J Z $\overline{B}$ $\overline{D}$ $\overline{M}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
III		J U Y $\overline{B}$ $\overline{D}$ $\overline{M}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
IV		E J		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		E F		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		F $\overline{K}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		F H		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		$\overline{E}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		K $\overline{L}$ $\overline{N}$ $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		N $\overline{L}$ $\overline{M}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
XI		T $\overline{P}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XII		S $\overline{P}$		
	1	t t	$\overline{A}$	0
	2	f t	$\overline{A}$	−6
	3	t f	$\overline{A}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms ±5% between jacks H and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

145. Matrix Card Assembly 548222

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, E, F, H, J, K, $\overline{L}$, M, R, S, T, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548222 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J		
	1	t	D	0
	2	f	D	−6
II		J Z $\overline{L}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		J Z $\overline{L}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IV		Z $\overline{L}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		W $\overline{A}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VI		H X $\overline{B}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		S X $\overline{F}$ $\overline{N}$ $\overline{T}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
VIII		J X $\overline{B}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		X $\overline{B}$ $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		F T		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XI		E L		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XII		E F		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XIII		L T		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XIV		$\overline{M}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XV		K Y		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XVI		M R		
	1	t t	P	0
	2	f t	P	−6
	3	t f	P	−6
XVII		B R		
	1	t t	P	0
	2	f t	P	−6
	3	t f	P	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

146. Matrix Card Assembly 548224

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, H, J, K, N, P, R, S, T, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548224 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F J $\overline{E}$ $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		F J $\overline{M}$ $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		F $\overline{R}$ $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		F S $\overline{B}$ $\overline{F}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		K		
	1	t	V	0
	2	f	V	−6
VI		$\overline{N}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VII		X Y		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		J		
	1	t	W	0
	2	f	W	−6
IX		T		
	1	t	W	0
	2	f	W	−6
X		N		
	1	t	W	0
	2	f	W	−6
XI		R		
	1	t	W	0
	2	f	W	−6
XII		N R $\overline{A}$ $\overline{H}$		
	1	t t t t	$\overline{S}$	0
	2	f t t t	$\overline{S}$	−6
	3	t f t t	$\overline{S}$	−6
	4	t t f t	$\overline{S}$	−6
	5	t t t f	$\overline{S}$	−6
XIII		H Z		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIV		P $\overline{N}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

147. Matrix Card Assembly 548226

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches C, E, F, H, J, K, L, M, N, S, U, Z, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548226 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E K Z $\overline{E}$ $\overline{F}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
II		K Z $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		K S Z $\overline{P}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IV		J K Z $\overline{P}$		
	1	t t t t	W	0
	2	f t t t	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
V		C U		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		F H $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		F J $\overline{E}$ $\overline{H}$ $\overline{N}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		F $\overline{K}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		F S $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		N U		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		H L $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		L $\overline{E}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIII		J L $\overline{L}$ $\overline{N}$ $\overline{P}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XIV		L S $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XV		$\overline{W}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XVI		M		
	1	t	B	0
	2	f	B	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

148. Matrix Card Assembly 548228

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, K, R, T, Y, $\overline{H}$, J, $\overline{K}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548228 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R Y		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		$\overline{K}$		
	1	t	V	0
	2	f	V	−6
III		K Y $\overline{K}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
IV		K $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		K T Y $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VI		F K $\overline{S}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VII		$\overline{J}$ $\overline{U}$		
	1	t t	$\overline{R}$	0
	2	f t	$\overline{R}$	−6
	3	t f	$\overline{R}$	−6
VIII		T $\overline{U}$		
	1	t t	$\overline{R}$	0
	2	f t	$\overline{R}$	−6
	3	t f	$\overline{R}$	−6
IX		$\overline{H}$ $\overline{P}$		
	1	t t	$\overline{R}$	0
	2	f t	$\overline{R}$	−6
	3	t f	$\overline{R}$	−6
X		F K $\overline{T}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		R T $\overline{J}$ $\overline{S}$		
	1	t t t t	$\overline{E}$	0
	2	f t t t	$\overline{E}$	−6
	3	t f t t	$\overline{E}$	−6
	4	t t f t	$\overline{E}$	−6
	5	t t t f	$\overline{E}$	−6
XII		F K $\overline{K}$ $\overline{T}$		
	1	t t t t	E	0
	2	f t t t	E	−6
	3	t f t t	E	−6
	4	t t f t	E	−6
	5	t t t f	E	−6
XIII		K T $\overline{J}$ $\overline{S}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
XIV		F K Y $\overline{J}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

149. Matrix Card Assembly 548229

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, K, M, P, R, Y, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548229 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Y $\overline{J}$ $\overline{S}$		
	1	t t t	E	0
	2	f t t	E	−6
	3	t f t	E	−6
	4	t t f	E	−6
II		Y $\overline{E}$ $\overline{J}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
III		H Y $\overline{J}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
IV		Y $\overline{J}$ $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		Y $\overline{F}$ $\overline{J}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VI		K Y $\overline{J}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VII		R Y $\overline{J}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		M		
	1	t	C	0
	2	f	C	−6
IX		J		
	1	t	V	0
	2	f	V	−6
X		M		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XI		J		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XII		P Y $\overline{J}$		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

150. Matrix Card Assembly 548231

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, P, R, S, T, Y, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548231 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S Y $\overline{P}$		
	1	t t t	E	0
	2	f t t	E	−6
	3	t f t	E	−6
	4	t t f	E	−6
II		S Y $\overline{E}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
III		F S Y		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
IV		P S Y		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6
V		S Y $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		S Y $\overline{F}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VII		H S Y		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VIII		R S Y		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		S Y $\overline{S}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
X		S Y $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		J Y $\overline{J}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
XII		T Y $\overline{J}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

151. Matrix Card Assembly 548233

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, P, R, S, $\overline{E}$, $\overline{F}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548233 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{S}$ $\overline{T}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		$\overline{E}$ $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		H $\overline{T}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		P $\overline{T}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		$\overline{R}$ $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		$\overline{F}$ $\overline{T}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		$\overline{M}$ $\overline{N}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VIII		J $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		F J S $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		J K R $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

152. Matrix Card Assembly 548235

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, P, R, S, T, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548235 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E $\overline{T}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
II		S $\overline{T}$		
	1	t t	$\overline{B}$	0
	2	f t	$\overline{B}$	−6
	3	t f	$\overline{B}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		$\overline{P}$ T		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
V		$\overline{E}$ T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
		F $\overline{T}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VI		P $\overline{T}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		$\overline{R}$ T		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		$\overline{F}$ T		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		H $\overline{T}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
		R $\overline{T}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		$\overline{S}$ T		
	1	t t	K	0
	2	f t	K	−6
	3	t f	K	−6
XII		H $\overline{T}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
XIII		J $\overline{T}$		
	1	t t	$\overline{N}$	0
	2	f t	$\overline{N}$	−6
	3	t f	$\overline{N}$	−6
XIV		T $\overline{T}$		
	1	t t	$\overline{A}$	0
	2	f t	$\overline{A}$	−6
	3	t f	$\overline{A}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

153. Matrix Card Assembly 548237

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, R, S, U, X, Y, $\overline{A}$, $\overline{D}$, $\overline{E}$, F, H, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548237 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L N S		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		S U X		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
III		S X $\overline{A}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
IV		K $\overline{L}$ $\overline{N}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		F Y $\overline{F}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		R Y $\overline{D}$ $\overline{F}$ $\overline{H}$ $\overline{S}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
VII		M		
	1	t	V	0
	2	f	V	−6
VIII		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		H K $\overline{L}$ $\overline{S}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
X		F Y $\overline{F}$ $\overline{H}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
XI		R Y $\overline{F}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
XII		K $\overline{E}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XIII		J $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and $\overline{A}$, $\overline{Y}$, and L, $\overline{Y}$ and N, $\overline{Y}$ and U, and $\overline{Y}$ and X.

j. Remove the matrix assembly from the test jack.

154. Matrix Card Assembly 548239

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, K, L, M, N, P, R, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks T and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548239 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		K P $\overline{R}$ $\overline{S}$		
	1	t t t t	T	0
	2	f t t t	T	−6
	3	t f t t	T	−6
	4	t t f t	T	−6
	5	t t t f	T	−6
I		M Y Z		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		M $\overline{B}$ $\overline{N}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
V		M Y $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		M Z $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		P $\overline{K}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VII		$\overline{E}$ $\overline{K}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VIII		$\overline{L}$ $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		F P $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		R $\overline{E}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XI		E L N		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XII		E U X		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XIII		E X $\overline{A}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XIV		K		
	1	t	W	0
	2	f	W	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

155. Matrix Card Assembly 548241

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches H, J, K, N, P, R, S, T, $\overline{E}$, $\overline{F}$, J, $\overline{P}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548241 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N		
	1	t	U	0
	2	f	U	−6
II		J		
	1	t	U	0
	2	f	U	−6
III		$\overline{U}$		
	1	t	U	0
	2	f	U	−6
IV		T $\overline{E}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
V		H $\overline{P}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
VI		J		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
VII		R		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VIII		N		
	1	t	C	0
	2	f	C	−6
IX		S $\overline{U}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		H $\overline{E}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		K P $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
XII		S		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIII		$\overline{P}$		
	1	t	D	0
	2	f	D	−6
XIV		$\overline{E}$		
	1	t	W	0
	2	f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

156. Matrix Card Assembly 548243

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches J, K, S, T, J, $\overline{K}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548243 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
II		S		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		$\overline{S}$		
	1	t	C	0
	2	f	C	−6
IV		J		
	1	t	V	0
	2	f	V	−6
V		J		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
VI		T		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VII		$\overline{T}$		
	1	t	D	0
	2	f	D	−6
VIII		$\overline{K}$		
	1	t	W	0
	2	f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks H and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

157. Matrix Card Assembly 548245

Note. The schematic diagram is in TM 11-5840-271-30/20 *and* TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, P, T, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548245 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K P $\overline{S}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		H J L $\overline{P}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
III		F K $\overline{K}$ $\overline{T}$		
	1	t t t t	X	0
	2	f t t t	X	−6
	3	t f t t	X	−6
	4	t t f t	X	−6
	5	t t t f	X	−6
IV		K P $\overline{S}$ $\overline{T}$		
	1	t t t t	E	0
	2	f t t t	E	−6
	3	t f t t	E	−6
	4	t t f t	E	−6
	5	t t t f	E	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		F		
	1	t	W	0
	2	f	W	−6
VI		$\overline{J}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VII		L		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
VIII		T		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IX		$\overline{R}$		
	1	t	D	0
	2	f	D	−6
X		$\overline{H}$		
	1	t	V	0
	2	f	V	−6
XI		$\overline{N}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks R and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

158. Matrix Card Assembly 548247

Note. The schematic diagram is in TM 11–5840–271–30/20 *and* TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, K, P, R, S, $\overline{F}$, $\overline{K}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548247 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P		
	1	t	C	0
	2	f	C	−6
II		F		
	1	t	W	0
	2	f	W	−6
III		F $\overline{K}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		F $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		F S $\overline{S}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		F K $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		F K $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VIII		F K $\overline{S}$ T		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		F K $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{E}$	0
	2	f t t t	$\overline{E}$	−6
	3	t f t t	$\overline{E}$	−6
	4	t t f t	$\overline{E}$	−6
	5	t t t f	$\overline{E}$	−6
X		F K $\overline{F}$ $\overline{S}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
XI		P S $\overline{K}$ $\overline{T}$		
	1	t t t t	$\overline{B}$	0
	2	f t t t	$\overline{B}$	−6
	3	t f t t	$\overline{B}$	−6
	4	t t f t	$\overline{B}$	−6
	5	t t t f	$\overline{B}$	−6
XII		R		
	1	t	E	0
	2	f	E	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test rack.

i. Return all TRUE-FALSE switches to neutral positions.

159. Matrix Card Assembly 548250

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, P, R, S, T, W, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548250 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K S $\overline{P}$ $\overline{H}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
II		J M $\overline{E}$ $\overline{H}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
III		J L $\overline{P}$ $\overline{H}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		Z $\overline{R}$ $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		S $\overline{E}$ $\overline{F}$ $\overline{H}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VI		$\overline{S}$ $\overline{T}$ $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		F $\overline{T}$ $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		T J $\overline{K}$ $\overline{H}$		
	1	t t t t	$\overline{D}$	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		$\overline{L}$ $\overline{H}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		R $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		F J $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		T $\overline{K}$ $\overline{T}$ $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XIII		$\overline{H}$ $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIV		N $\overline{A}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
XV		H P $\overline{V}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
XVI		P $\overline{F}$ $\overline{V}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
XVII		P $\overline{N}$ $\overline{R}$ $\overline{U}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6
XVIII		E		
	1	t	$\overline{X}$	0
	2	f	$\overline{X}$	−6
XIX		J $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XX		T $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XXI		D W		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XXII		$\overline{M}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

160. Matrix Card Assembly 548251

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, K, L, N, P, R, S, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548251 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false).

Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P $\overline{M}$		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
II		$\overline{M}$ $\overline{P}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
III		H $\overline{M}$		
	1	t t	E	0
	2	f t	E	−6
	3	t f	E	−6
IV		$\overline{H}$ $\overline{M}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
V		R $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		$\overline{M}$ $\overline{R}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VII		J $\overline{M}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		$\overline{J}$ $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		K $\overline{M}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		$\overline{K}$ $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		L $\overline{M}$		
	1	t t	F	0
	2	f t	F	−6
	3	t f	F	−6
XII		$\overline{L}$ $\overline{M}$		
	1	t t	$\overline{F}$	0
	2	f t	$\overline{F}$	−6
	3	t f	$\overline{F}$	−6
XIII		N $\overline{M}$		
	1	t t	T	0
	2	f t	T	−6
	3	t f	T	−6
XIV		$\overline{M}$ $\overline{N}$		
	1	t t	$\overline{T}$	0
	2	f t	$\overline{T}$	−6
	3	t f	$\overline{T}$	−6
XV		S $\overline{M}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVI		$\overline{M}$ $\overline{S}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

161. Matrix Card Assembly 548253

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, D, E, F, H, J, K, L, M, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks W and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548253 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P Z $\overline{A}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		Z $\overline{A}$ $\overline{E}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		S Z $\overline{A}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		E T U X $\overline{B}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
V		F L R		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VI		K		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VII		F L $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		H		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IX		$\overline{M}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
X		J Y $\overline{H}$ J $\overline{K}$ $\overline{L}$ $\overline{V}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t f t t t t t	$\overline{D}$	−6
	4	t t f t t t t	$\overline{D}$	−6
	5	t t t f t t t	$\overline{D}$	−6
	6	t t t t f t t	$\overline{D}$	−6
	7	t t t t t f t	$\overline{D}$	−6
	8	t t t t t t f	$\overline{D}$	−6
XI		D M $\overline{W}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XII		C J Y $\overline{H}$ J $\overline{K}$ $\overline{L}$		
	1	t t t t t t t	W	0
	2	f t t t t t t	W	−6
	3	t f t t t t t	W	−6
	4	t t f t t t t	W	−6
	5	t t t f t t t	W	−6
	6	t t t t f t t	W	−6
	7	t t t t t f t	W	−6
	8	t t t t t t f	W	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks $\overline{Y}$ and F, $\overline{Y}$ and N, $\overline{Y}$ and $\overline{R}$, $\overline{Y}$ and S, $\overline{Y}$ and $\overline{S}$, $\overline{Y}$ and $\overline{T}$, $\overline{Y}$ and $\overline{U}$.

l. Remove the matrix assembly from the test jack.

162. Matrix Card Assembly 548256

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, L, N, X, Y, Z, $\overline{E}$, $\overline{F}$, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548256 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		X		
	1	t	C	0
	2	f	C	−6
I		Z		
	1	t	V	0
	2	f	V	−6
II		L X[a]		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IV		Y $\overline{P}$[a]		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
V		E Y $\overline{F}$[a]		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		$\overline{S}$[b]		
	1	t	D	0
	2	f	D	−6
VII		L Z		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		H Y $\overline{E}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IX		Y $\overline{E}$ $\overline{R}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
X		$\overline{F}$		
	1	t	W	0
	2	f	W	−6
XI		Y $\overline{E}$ $\overline{S}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XII		$\overline{K}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XIII		T		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIV		$\overline{U}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XV		N		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XVI		J[b]		
	1	t	D	0
	2	t	D	−6

[a] Set TRUE-FALSE switch J to TRUE.
[b] Set TRUE-FALSE switches L and X to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

163. Matrix Card Assembly 548258

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, S, T, X, Y, $\overline{A}$, $\overline{B}$, F, $\overline{H}$, J, $\overline{K}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548258 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E $\overline{H}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
II		E J		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
III		E $\overline{S}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		T		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
V		N		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VI		H $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		$\overline{H}$ $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VIII		J $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IX		$\overline{R}$ $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		J		
	1	t	V	0
	2	f	V	−6
XI		N		
	1	t	V	0
	2	f	V	−6
XII		$\overline{B}$ $\overline{K}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XIII		F N		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XIV		$\overline{F}$		
	1	t	W	0
	2	f	W	−6
XV		L S X $\overline{A}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVI		P S Y		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XVII		K		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

164. Matrix Card Assembly 548260

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, J, L, N, R, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks W and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548260 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L X Z $\overline{A}$ $\overline{K}$ $\overline{M}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
II		L R X $\overline{K}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		F L N U Z $\overline{H}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
IV		F L U Z $\overline{N}$ $\overline{U}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
V		U $\overline{B}$ $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VI		L $\overline{L}$ $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VII		J Y Z $\overline{M}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		J R Y		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IX		Y $\overline{L}$ $\overline{P}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
X		L X Z $\overline{A}$ $\overline{M}$ $\overline{T}$		
	1	t t t t t t	W	0
	2	f t t t t t	W	−6
	3	t f t t t t	W	−6
	4	t t f t t t	W	−6
	5	t t t f t t	W	−6
	6	t t t t f t	W	−6
	7	t t t t t f	W	−6
XI		L R X $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

165. Matrix Card Assembly 548262

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, K, L, N, P, R, U, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, J, $\overline{L}$, $\overline{M}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548262 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E F L U Z		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6
II		L $\overline{J}$ $\overline{L}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
III		P Y Z $\overline{M}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IV		P R Y		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
V		Y $\overline{E}$ $\overline{L}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VI		L U X Z $\overline{M}$ $\overline{R}$ $\overline{U}$		
	1	t t t t t t t	$\overline{V}$	0
	2	f t t t t t t	$\overline{V}$	−6
	3	t f t t t t t	$\overline{V}$	−6
	4	t t f t t t t	$\overline{V}$	−6
	5	t t t f t t t	$\overline{V}$	−6
	6	t t t t f t t	$\overline{V}$	−6
	7	t t t t t f t	$\overline{V}$	−6
	8	t t t t t t f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		U Y $\overline{M}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VIII		U $\overline{B}$ $\overline{S}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
IX		L $\overline{L}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
X		L N X Z $\overline{M}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XI		Y $\overline{F}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XII		$\overline{B}$ $\overline{F}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIII		$\overline{F}$ $\overline{L}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIV		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

166. Matrix Card Assembly 548264

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, J, L, P, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, J, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548264 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J Y $\overline{L}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
II		Y $\overline{L}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		E L $\overline{B}$ $\overline{P}$[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		E Z $\overline{M}$ $\overline{P}$ $\overline{R}$[a]		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		P Y $\overline{B}$ $\overline{P}$[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		P Z $\overline{F}$ $\overline{M}$ $\overline{P}$[a]		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VII		L P $\overline{L}$ $\overline{P}$[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VIII		Y $\overline{F}$ J $\overline{L}$[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		L P $\overline{B}$ $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		P Z $\overline{E}$ $\overline{M}$ $\overline{R}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

[a] Set TRUE-FALSE switch J to TRUE.

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

167. Matrix Card Assembly 548266

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, L, P, U, X, Y, Z, B, $\overline{E}$, $\overline{F}$, J, $\overline{L}$, and $\overline{M}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks W and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548266 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		U $\overline{B}$ J		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
II		E Y $\overline{B}$ $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		E Z $\overline{E}$ $\overline{F}$ $\overline{M}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IV		E L $\overline{E}$ $\overline{L}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		F		
	1	t	V	0
	2	f	V	−6
VI		H P X Y $\overline{L}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

168. Matrix Card Assembly 548268

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, T, U, Z, $\overline{E}$, $\overline{H}$, J, $\overline{P}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548268 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
II		T $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		E F R		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		F H P		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		P R $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		H P $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		E R $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		E H $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		N		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XI		S		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XII		J L U Z $\overline{H}$ J $\overline{U}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

169. Matrix Card Assembly 548274

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches F, H, J, K, L, N, S, T, U, X, $\overline{A}$, $\overline{E}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, and $\overline{P}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548274 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F H T $\overline{A}$ $\overline{E}$ $\overline{H}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
II		F H L $\overline{A}$ $\overline{H}$ $\overline{P}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
III		F H S U $\overline{A}$ $\overline{H}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
IV		H K $\overline{A}$ $\overline{E}$ $\overline{H}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
V		H S $\overline{A}$ $\overline{H}$ $\overline{L}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VI		$\overline{H}$ $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		K		
	1	t	C	0
	2	f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		L		
	1	t	C	0
	2	f	C	−6
IX		$\overline{H}$ $\overline{M}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
X		$\overline{K}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XI		J N X $\overline{N}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks E, T, $\overline{F}$, $\overline{S}$, and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

170. Matrix Card Assembly 548276

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, L, N, P, R, T, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548276 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J Z $\overline{J}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		H $\overline{T}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
III		F L T $\overline{L}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		N $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		Y $\overline{R}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		E Y		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		$\overline{H}$		
	1	t	W	0
	2	f	W	−6
VIII		J T $\overline{N}$		
	1	t t t	B	0
	2	f t t	B	−6
	3	t f t	B	−6
	4	t t f	B	−6
IX		J T $\overline{K}$		
	1	t t t	B	0
	2	f t t	B	−6
	3	t f t	B	−6
	4	t t f	B	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		$\overline{\Pi}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XI		P U $\overline{A}$ $\overline{M}$ $\overline{U}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XII		R Y $\overline{B}$ $\overline{E}$ $\overline{F}$ $\overline{U}$		
	1	t t t t t t	$\overline{C}$	0
	2	f t t t t t	$\overline{C}$	−6
	3	t f t t t t	$\overline{C}$	−6
	4	t t f t t t	$\overline{C}$	−6
	5	t t t f t t	$\overline{C}$	−6
	6	t t t t f t	$\overline{C}$	−6
	7	t t t t t f	$\overline{C}$	−6
XIII		R Y $\overline{B}$ $\overline{P}$ $\overline{S}$ $\overline{U}$		
	1	t t t t t t	$\overline{C}$	0
	2	f t t t t t	$\overline{C}$	−6
	3	t f t t t t	$\overline{C}$	−6
	4	t t f t t t	$\overline{C}$	−6
	5	t t t f t t	$\overline{C}$	−6
	6	t t t t f t	$\overline{C}$	−6
	7	t t t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and S.

j. Remove the matrix assembly from the test jack.

171. Matrix Card Assembly 548278

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches C, E, F, H, J, K, L, N, P, R, S, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548278 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
II		C Z $\overline{C}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		C H		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		H $\overline{P}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
V		U $\overline{W}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		U $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		$\overline{K}$ $\overline{S}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		J $\overline{S}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{A}$ $\overline{B}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		W $\overline{A}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		J $\overline{E}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		R $\overline{E}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		E L N $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XIV		E F K $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XV		E $\overline{T}$ $\overline{U}$ $\overline{V}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XVI		E $\overline{F}$ $\overline{R}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XVII		U $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XVIII		$\overline{H}$ $\overline{S}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIX		Y $\overline{A}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XX		P $\overline{E}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XXI		H X $\overline{N}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

172. Matrix Card Assembly 548280

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548280 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false).

Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E S U $\overline{M}$ $\overline{R}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
II		M $\overline{F}$[a]		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
III		H $\overline{E}$[a]		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IV		F $\overline{B}$[a]		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
V		N		
	1	t	V	0
	2	f	V	−6
VI		X $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		X $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		$\overline{K}$		
	1	t	W	0
	2	f	W	−6
IX		J T Z		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
X		$\overline{A}$ $\overline{K}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		$\overline{K}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XII		L P R $\overline{P}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
XIII		K L P $\overline{H}$ $\overline{M}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
XIV		R Y $\overline{J}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XV		K Y $\overline{H}$ J $\overline{M}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

[a] Set TRUE-FALSE switches U, $\overline{M}$, and $\overline{R}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

173. Matrix Card Assembly 548282

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, K, L, M, N, P, R, S, T, U, V, X, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548282 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		E S $\overline{E}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
I		E K $\overline{P}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
II		E P		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
V		F R		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
V		X $\overline{T}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VI		H $\overline{J}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		U T		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		$\overline{M}$ $\overline{S}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		$\overline{A}$ $\overline{K}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		X $\overline{A}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XI		$\overline{R}$		
	1	t	W	0
	2	f	W	−6
XII		$\overline{M}$ $\overline{U}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIII		N $\overline{F}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIV		X $\overline{E}$ $\overline{U}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XV		L V X $\overline{U}$		
	1	t t t t	W	0
	2	f t t t	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XVI		K X $\overline{U}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XVII		Z $\overline{H}$ $\overline{N}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

174. Matrix Card Assembly 548284

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches B, C, D, E, F, H, K, L, M, N, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jack W and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548284 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{E}$		
	1	t	V	0
	2	f	V	−6
II		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
III		H		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IV		F U X $\overline{A}$ $\overline{F}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
V		F U X $\overline{B}$ $\overline{S}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
VI		$\overline{T}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VII		T $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		L R T		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		$\overline{U}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		E Z		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		D S $\overline{B}$ $\overline{N}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		B M S $\overline{B}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XIII		$\overline{A}$ $\overline{K}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIV		Y $\overline{V}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XV		N Y		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVI		C Y		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVII		J $\overline{L}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVIII		R $\overline{K}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIX		$\overline{H}$ $\overline{K}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XX		Y $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jack $\overline{Y}$ and jacks J and $\overline{P}$.

l. Remove the matrix assembly from the test jack.

175. Matrix Card Assembly 548287

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches B, E, F, H, J, K, L, M, N, P, R, S, T, U, X, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548287 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J $\overline{E}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		K		
	1	t	V	0
	2	f	V	−6
III		E H T $\overline{H}$ J		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		E H T $\overline{L}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		E F T $\overline{M}$ $\overline{S}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VI		B R $\overline{F}$ $\overline{H}$ $\overline{X}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VII		F T $\overline{K}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VIII		L $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		L P		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		$\overline{E}$ $\overline{N}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XI		K		
	1	t	W	0
	2	f	W	−6
XII		E S X $\overline{L}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t t	W	0
	2	f t t t t t	W	−6
	3	t f t t t t	W	−6
	4	t t f t t t	W	−6
	5	t t t f t t	W	−6
	6	t t t t f t	W	−6
	7	t t t t t f	W	−6
XIII		B R S $\overline{A}$ H $\overline{X}$		
	1	t t t t t t	W	0
	2	f t t t t t	W	−6
	3	t f t t t t	W	−6
	4	t t f t t t	W	−6
	5	t t t f t t	W	−6
	6	t t t t f t	W	−6
	7	t t t t t f	W	−6
XIV		M U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XV		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XVI		N $\overline{E}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XVII		N $\overline{U}$		
	1	t t	$\overline{D}$	0

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

176. Matrix Card Assembly 548289

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, K, L, M, N, P, R, T, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548289 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K M		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		L N R $\overline{B}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		T		
	1	t	V	0
	2	f	V	−6
IV		K Z		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		E K		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		K P		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		K $\overline{F}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		K $\overline{R}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IX		K $\overline{E}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
X		K $\overline{U}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and F, $\overline{Y}$ and H, $\overline{Y}$ and S, $\overline{Y}$ and U, $\overline{Y}$ and $\overline{H}$, $\overline{Y}$ and J, $\overline{Y}$ and $\overline{S}$, and $\overline{Y}$ and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

177. Matrix Card Assembly 548291

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, J, K, L, M, N, P, S, U, W, X, Y, Z, $\overline{A}$, B, $\overline{C}$, D, $\overline{F}$, H, J, $\overline{K}$, $\overline{L}$, and $\overline{N}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548291 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J $\overline{D}$ $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		J Z		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		S $\overline{D}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		P W $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		M J $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		M $\overline{H}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		K M $\overline{K}$ $\overline{L}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		K M $\overline{H}$ $\overline{L}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		N X $\overline{C}$ $\overline{L}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		L N W X		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		E N U X		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XII		E N Y $\overline{A}$ $\overline{B}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

178. Matrix Card Assembly 548292

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, J, N, S, T, U, W, Y, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, H, J, $\overline{L}$, $\overline{M}$, $\overline{N}$, P, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548292 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N $\overline{D}$ $\overline{L}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		N $\overline{D}$ $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		D N W $\overline{D}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		E T Y $\overline{A}$ $\overline{B}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		N $\overline{D}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		J N $\overline{D}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		N Y $\overline{A}$ $\overline{D}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		N U $\overline{D}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		S T U $\overline{C}$ $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
X		T $\overline{H}$ $\overline{L}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		T $\overline{D}$ $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		T Y $\overline{A}$ $\overline{D}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XIII		T $\overline{H}$ $\overline{L}$ $\overline{P}$ $\overline{R}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jacks.

k. Return all TRUE-FALSE switches to neutral positions.

179. Matrix Card Assembly 548294

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, H, J, K, L, M, N, P, T, U, W, X, Y, $\overline{C}$, $\overline{D}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 selector switch to position 8.

e. Insert matrix assembly 548294 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		T W $\overline{D}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		E T U $\overline{H}$ $\overline{M}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
III		T $\overline{H}$ J $\overline{M}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		J T $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		L T $\overline{H}$ $\overline{L}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		P U X $\overline{C}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		U X $\overline{H}$ $\overline{M}$ $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		D H K L P X $\overline{C}$ J $\overline{S}$		
	1	t t t t t t t t t	V	0
	2	f t t t t t t t t	V	−6
	3	t f t t t t t t t	V	−6
	4	t t f t t t t t t	V	−6
	5	t t t f t t t t t	V	−6
	6	t t t t f t t t t	V	−6
	7	t t t t t f t t t	V	−6
	8	t t t t t t f t t	V	−6
	9	t t t t t t t f t	V	−6
	10	t t t t t t t t f	V	−6
IX		E M X Y $\overline{F}$ $\overline{H}$ J $\overline{N}$		
	1	t t t t t t t t	V	0
	2	f t t t t t t t	V	−6
	3	t f t t t t t t	V	−6
	4	t t f t t t t t	V	−6
	5	t t t f t t t t	V	−6
	6	t t t t f t t t	V	−6
	7	t t t t t f t t	V	−6
	8	t t t t t t f t	V	−6
	9	t t t t t t t f	V	−6
X		N $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks $\overline{U}$ and $\overline{Y}$.

l. Remove the matrix assembly from the test jack.

180. Matrix Card Assembly 548296

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches B, E, F, J, K, L, M, N, P, R, S, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{W}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548296 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J K		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		K $\overline{E}$ $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		N		
	1	t	V	0
	2	f	V	−6
IV		F S Y Z $\overline{P}$[a]		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
V		P S $\overline{A}$ $\overline{M}$[a]		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
VI		$\overline{B}$ $\overline{F}$[a]		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		$\overline{F}$ T^a		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VIII		M $\overline{F}^a$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IX		L U $\overline{F}$ $\overline{J}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
X		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XI		X		
	1	t	W	0
	2	f	W	−6
XII		E K R $\overline{K}$ $\overline{L}$ $\overline{N}$ $\overline{S}$ $\overline{U}$ $\overline{W}$		
	1	t t t t t t t t t	D	0
	2	f t t t t t t t t	D	−6
	3	t f t t t t t t t	D	−6
	4	t t f t t t t t t	D	−6
	5	t t t f t t t t t	D	−6
	6	t t t t f t t t t	D	−6
	7	t t t t t f t t t	D	−6
	8	t t t t t t f t t	D	−6
	9	t t t t t t t f t	D	−6
	10	t t t t t t t t f	D	−6
XIII		B K $\overline{D}$ $\overline{U}$ $\overline{X}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6

[a] Set TRUE-FALSE switches L and J to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and H, and $\overline{Y}$ and T.

j. Remove the matrix assembly from the test jack.

181. Matrix Card Assembly 548298

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, J, K, N, T, U, Y, $\overline{F}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548298 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
II		J U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
III		Y		
	1	t	D	0
	2	f	D	−6
IV		F N T $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		K		
	1	t	V	0
	2	f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		K $\overline{F}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VII		K $\overline{R}$		
	1	t f	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and E, $\overline{Y}$ and H, $\overline{Y}$ and R, $\overline{Y}$ and $\overline{E}$, $\overline{Y}$ and $\overline{F}$, $\overline{Y}$ and $\overline{K}$, $\overline{Y}$ and $\overline{P}$, and $\overline{Y}$ and $\overline{R}$.

j. Remove the matrix assembly from the test jack.

182. Matrix Card Assembly 548300

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches F, H, J, K, P, T, V, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{H}$, J, $\overline{L}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548300 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{U}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
II		H		
	1	t	E	0
	2	f	E	−6
III		$\overline{T}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
IV		J		
	1	t	W	0
	2	f	W	−6
V		$\overline{S}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
VI		$\overline{J}$		
	1	t	$\overline{X}$	0
	2	f	$\overline{X}$	−6
VII		Y $\overline{A}$ $\overline{P}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VIII		F $\overline{B}$ $\overline{L}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
IX		V Z $\overline{R}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
X		K T $\overline{H}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks H, J, P, S, $\overline{T}$, J, $\overline{N}$, and $\overline{S}$.

j. Remove the matrix assembly from the test jack.

183. Matrix Card Assembly 548302

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches E, H, J, L, N, S, U, $\overline{E}$, F, $\overline{H}$, J, K, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548302 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{H}$		
	1	t	X	0
	2	f	X	−6
II		$\overline{E}$		
	1	t	$\overline{C}$, V, W	0
	2	f	$\overline{C}$, V, W	−6
III		$\overline{T}$		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
IV		S $\overline{K}$		
	1	t t	$\overline{B}$	0
	2	f t	$\overline{B}$	−6
	3	t f	$\overline{B}$	−6
V		J $\overline{J}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		J L		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VII		E		
	1	t	D	0
	2	f	D	−6
VIII		U		
	1	t	D	0
	2	f	D	−6
IX		$\overline{F}$		
	1	t	D, $\overline{D}$	0
	2	f	D, $\overline{D}$	−6
X		N		
	1	t	V, $\overline{W}$	0
	2	f	V, $\overline{W}$	−6
XI		$\overline{S}$		
	1	t	V, $\overline{W}$	0
	2	f	V, $\overline{W}$	−6
XII		H		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

184. Matrix Card Assembly 548304

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, F, H, J, K, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{W}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks $\overline{C}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548304 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
		M T X $\overline{N}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
I		H K $\overline{J}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		H P R		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		H U $\overline{F}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
		M X $\overline{M}$ $\overline{U}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
I		$\overline{B}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
II		L M X		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		$\overline{A}$ $\overline{K}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{E}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
X		Y $\overline{P}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XI		F $\overline{L}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XII		$\overline{R}$ $\overline{W}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XIII		B $\overline{H}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XIV		J Z $\overline{M}$ $\overline{X}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
XV		J N $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XVI		J $\overline{S}$ $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XVII		J		
	1	t	V	0
	2	f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVIII		$\overline{E}$		
	1	t	W	0
	2	f	W	−6
XIX		J S		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

185. Matrix Card Assembly 548306

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches C, D, E, F, H, L, S, X, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548306 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F H $\overline{A}$ $\overline{K}$ $\overline{P}$ $\overline{R}$		
	1	t t t t t t	$\overline{C}$	0
	2	f t t t t t	$\overline{C}$	−6
	3	t f t t t t	$\overline{C}$	−6
	4	t t f t t t	$\overline{C}$	−6
	5	t t t f t t	$\overline{C}$	−6
	6	t t t t f t	$\overline{C}$	−6
	7	t t t t t f	$\overline{C}$	−6
II		$\overline{B}$ $\overline{K}$ $\overline{N}$ $\overline{P}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t t	$\overline{C}$ $\overline{C}$	−6
	4	t t f t	$\overline{C}$ $\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		$\overline{D}$ $\overline{K}$ $\overline{N}$ $\overline{P}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t t	$\overline{C}$ $\overline{C}$	−6
	4	t t f t	$\overline{C}$ $\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IV		J $\overline{K}$ $\overline{N}$ $\overline{P}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t t	$\overline{C}$ $\overline{C}$	−6
	4	t t f t	$\overline{C}$ $\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
V		$\overline{E}$ $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$ $\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VI		L $\overline{F}$ $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t	$\overline{C}$ $\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		S $\overline{E}$ $\overline{F}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t	$\overline{C}$ $\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		D E $\overline{L}$ $\overline{M}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t t	$\overline{C}$ $\overline{C}$	−6
	4	t t f t	$\overline{C}$ $\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IX		D E X $\overline{L}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		D E $\overline{L}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XI		C E $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		E S Z $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XIII		$\overline{T}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XIV		$\overline{H}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks E and $\overline{P}$.

j. Remove the matrix assembly from the test jack.

186. Matrix Card Assembly 548308

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches K, N, R, S, T, X, Y, Z, $\overline{A}$, $\overline{F}$, $\overline{H}$, $\overline{M}$, $\overline{N}$, and $\overline{P}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548308 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K		
	1	t	C	0
	2	f	C	−6
II		X		
	1	t	D	0
	2	f	D	−6
III		Z		
	1	t	E	0
	2	f	E	−6
IV		$\overline{A}$		
	1	t	L	0
	2	f	L	−6
V		S		
	1	t	J	0
	2	f	J	−6
VI		Y		
	1	t	U	0
	2	f	U	−6
VII		Z		
	1	t	V	0
	2	f	V	−6
VIII		X		
	1	t	W	0
	2	f	W	−6
IX		R		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		$\overline{A}$		
	1	t	$\overline{D}, \overline{E}$	0
	2	f	$\overline{D}, \overline{E}$	−6
XI		N		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XII		K T $\overline{H}$ $\overline{P}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XIII		$\overline{N}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XIV		$\overline{M}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XV		$\overline{F}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XVI		Z		
	1	t	H	0
	2	f	H	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

187. Matrix Card Assembly 548310

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches R, S, T, Y, Z, $\overline{A}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548310 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{F}$		
	1	t	C	0
	2	f	C	−6
II		T		
	1	t	D	0
	2	f	D	−6
III		R		
	1	t	E, $\overline{V}$	0
	2	f	E, $\overline{V}$	−6
IV		$\overline{H}$		
	1	t	U	0
	2	f	U	−6
V		S		
	1	t	V	0
	2	f	V	−6
VI		Y		
	1	t	W	0
	2	f	W	−6
VII		T		
	1	t	X	0
	2	f	X	−6
VIII		$\overline{A}$		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
IX		Z		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
X		$\overline{K}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		J		
	1	t	E, U	0
	2	f	E, U	−6
XII		R		
	1	t	W	0
	2	f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

188. Matrix Card Assembly 548312

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, K, N, P, R, S, T, Y, Z, A, F, H, M, P, and R to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548312 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Z		
	1	t	D	0
	2	f	D	−6
II		S		
	1	t	E	0
	2	f	E	−6
III		P		
	1	t	U	0
	2	f	U	−6
IV		T		
	1	t	V	0
	2	f	V	−6
V		S		
	1	t	W	0
	2	f	W	−6
VI		P		
	1	t	X	0
	2	f	X	−6
VII		N		
	1	t	X	0
	2	f	X	−6
VIII		R M		
	1	t t	B	0
	2	f t	B	−6
	3	t f	B	−6
IX		A		
	1	t	C, V	0
	2	f	C, V	−6
X		K T F H		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
XI		K Y H P		
	1	t t t t	E	0
	2	f t t t	E	−6
	3	t f t t	E	−6
	4	t t f t	E	−6
	5	t t t f	E	−6
XII		R		
	1	t	W	0
	2	f	W	−6
XIII		P		
	1	t	F	0
	2	f	F	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		H		
	1	t	C	0
	2	f	C	−6
XV		J		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

189. Matrix Card Assembly 548314

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, P, R, S, T, U, V, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{K}$, $\overline{L}$, $\overline{S}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548314 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K P V $\overline{L}$ $\overline{S}$		
	1	t t t t t	$\overline{R}$	0
	2	f t t t t	$\overline{R}$	−6
	3	t f t t t	$\overline{R}$	−6
	4	t t f t t	$\overline{R}$	−6
	5	t t t f t	$\overline{R}$	−6
	6	t t t t f	$\overline{R}$	−6
II		J K P V $\overline{S}$		
	1	t t t t t	$\overline{R}$	0
	2	f t t t t	$\overline{R}$	−6
	3	t f t t t	$\overline{R}$	−6
	4	t t f t t	$\overline{R}$	−6
	5	t t t f t	$\overline{R}$	−6
	6	t t t t f	$\overline{R}$	−6
III		F K P V $\overline{S}$		
	1	t t t t t	$\overline{R}$	0
	2	f t t t t	$\overline{R}$	−6
	3	t f t t t	$\overline{R}$	−6
	4	t t f t t	$\overline{R}$	−6
	5	t t t f t	$\overline{R}$	−6
	6	t t t t f	$\overline{R}$	−6
IV		D E K L $\overline{D}$		
	1	t t t t t	$\overline{R}$	0
	2	f t t t t	$\overline{R}$	−6
	3	t f t t t	$\overline{R}$	−6
	4	t t f t t	$\overline{R}$	−6
	5	t t t f t	$\overline{R}$	−6
	6	t t t t f	$\overline{R}$	−6
V		H K $\overline{T}$		
	1	t t t	$\overline{R}$	0
	2	f t t	$\overline{R}$	−6
	3	t f t	$\overline{R}$	−6
	4	t t f	$\overline{R}$	−6
VI		R T $\overline{K}$		
	1	t t t	$\overline{R}$	0
	2	f t t	$\overline{R}$	−6
	3	t f t	$\overline{R}$	−6
	4	t t f	$\overline{R}$	−6
VII		$\overline{A}$		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
VIII		M		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
IX		N U Y Z $\overline{B}$ $\overline{E}$ $\overline{F}$		
	1	t t t t t t t	$\overline{R}$	0
	2	f t t t t t t	$\overline{R}$	−6
	3	t f t t t t t	$\overline{R}$	−6
	4	t t f t t t t	$\overline{R}$	−6
	5	t t t f t t t	$\overline{R}$	−6
	6	t t t t f t t	$\overline{R}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	7	t t t t t f t	$\overline{R}$	−6
	8	t t t t t t f	$\overline{R}$	−6
X		X		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XI		U		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XII		W		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIII		$\overline{F}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIV		S		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XV		$\overline{V}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

190. Matrix Card Assembly 548316

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, R, S, T, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{S}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548316 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
II		S		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
III		W		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
IV		X		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
V		$\overline{F}$		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
VI		$\overline{V}$		
	1	t	$\overline{P}$	0
	2	f	$\overline{P}$	−6
VII		K N $\overline{H}$ $\overline{L}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		J K N $\overline{H}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		F K N $\overline{\text{M}}$ $\overline{\text{S}}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
X		H K $\overline{\text{N}}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		D E K L $\overline{\text{U}}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XII		T $\overline{\text{C}}$ $\overline{\text{K}}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		M		
	1	t	V	0
	2	f	V	−6
XIV		$\overline{\text{A}}$		
	1	t	V	0
	2	f	V	−6
XV		R W Y Z $\overline{\text{B}}$ $\overline{\text{E}}$ J		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

191. Matrix Card Assembly 548318

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, J, K, L, M, N, R, T, U, X, Y, Z, $\overline{\text{A}}$, $\overline{\text{B}}$, $\overline{\text{E}}$, $\overline{\text{F}}$, J, $\overline{\text{K}}$, $\overline{\text{L}}$, $\overline{\text{M}}$, $\overline{\text{U}}$, and $\overline{\text{V}}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548318 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{\text{F}}$ $\overline{\text{L}}$ $\overline{\text{U}}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		J $\overline{\text{F}}$ $\overline{\text{U}}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		F $\overline{\text{F}}$ $\overline{\text{U}}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		D E K L $\overline{\text{M}}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		T $\overline{F}$ $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		$\overline{A}$		
	1	t	V	0
	2	f	V	−6
VII		M		
	1	t	V	0
	2	f	V	−6
VIII		N R Y Z $\overline{B}$ $\overline{E}$ $\overline{J}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
IX		N		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
X		U		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XI		X		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XII		$\overline{E}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XIII		J		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XIV		$\overline{V}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{F}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

192. Matrix Card Assembly 548320

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{S}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548320 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S $\overline{L}$ $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		J S $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		F S $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		D E K L P		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		S T $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		$\overline{A}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VII		N U Y Z $\overline{B}$ $\overline{E}$ J		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
VIII		M		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		R		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
X		H		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XI		N		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XII		$\overline{E}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XIII		$\overline{V}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XIV		$\overline{J}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and S.

j. Remove the matrix assembly from the test jack.

193. Matrix Card Assembly 548322

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches N, R, S, U, W, X, $\overline{F}$, J, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548322 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R		
	1	t	T	0
	2	f	T	−6
II		S		
	1	t	T	0
	2	f	T	−6
III		W		
	1	t	T	0
	2	f	T	−6
IV		X		
	1	t	T	0
	2	f	T	−6
V		J		
	1	t	T	0
	2	f	T	−6
VI		$\overline{V}$		
	1	t	T	0
	2	f	T	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		N		
	1	t	L	0
	2	f	L	−6
VIII		S		
	1	t	L	0
	2	f	L	−6
IX		U		
	1	t	L	0
	2	f	L	−6
X		X		
	1	t	L	0
	2	f	L	−6
XI		$\overline{F}$		
	1	t	L	0
	2	f	L	−6
XII		$\overline{V}$		
	1	t	L	0
	2	f	L	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

194. Matrix Card Assembly 548324

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, L, M, N, P, R, S, U, W, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, J, $\overline{K}$, $\overline{L}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548324 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{A}$		
	1	t	V	0
	2	f	V	−6
II		M		
	1	t	V	0
	2	f	V	−6
III		P R S W Z $\overline{B}$ $\overline{F}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
IV		D E L $\overline{D}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		F N $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		J N $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		N $\overline{K}$ $\overline{L}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		H		
	1	t	K	0
	2	f	K	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		U		
	1	t	K	0
	2	f	K	6
X		W		
	1	t	K	0
	2	f	K	−6
XI		$\overline{E}$		
	1	t	K	0
	2	f	K	−6
XII		$\overline{J}$		
	1	t	K	0
	2	f	K	−6
XIII		$\overline{V}$		
	1	t	K	0
	2	f	K	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

195. Matrix Card Assembly 548326

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, H, K, L, M, P, R, S, U, W, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{L}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548326 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{C}$ $\overline{L}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		K $\overline{C}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		F $\overline{C}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		S U W Y Z $\overline{B}$ $\overline{F}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t f t t t t t	$\overline{D}$	−6
	4	t t f t t t t	$\overline{D}$	−6
	5	t t t f t t t	$\overline{D}$	−6
	6	t t t t f t t	$\overline{D}$	−6
	7	t t t t t f t	$\overline{D}$	−6
	8	t t t t t t f	$\overline{D}$	−6
V		M		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		D E L P		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		$\overline{A}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VIII		H		
	1	t	J	0
	2	f	J	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		R		
	1	t	J	0
	2	f	J	−6
X		W		
	1	t	J	0
	2	f	J	−6
XI		$\overline{E}$		
	1	t	J	0
	2	f	J	−6
XII		$\overline{T}$		
	1	t	J	0
	2	f	J	−6
XIII		$\overline{V}$		
	1	t	J	0
	2	f	J	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

196. Matrix Card Assembly 548328

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548328 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H K $\overline{L}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		H K $\overline{R}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		J K L $\overline{M}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		P T $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		$\overline{A}$		
	1	t	V	0
	2	f	V	−6
VI		M		
	1	t	V	0
	2	f	V	−6
VII		N R S Y Z $\overline{B}$ $\overline{F}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
VIII		$\overline{P}$		
	1	t	D	0
	2	f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{E}$		
	1	t	W	0
	2	f	W	−6
X		F		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XI		U		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XII		$\overline{H}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XIII		$\overline{S}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XIV		J		
	1	t	B	0
	2	f	B	−6
XV		$\overline{U}$		
	1	t	C	0
	2	f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all the TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks P and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

197. Matrix Card Assembly 548330

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548330 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N S U Y Z $\overline{B}$ $\overline{F}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
II		T $\overline{H}$ $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		J K L P		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IV		E K $\overline{N}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
V		$\overline{A}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VI		E K $\overline{L}$ $\overline{N}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VII		M		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		$\overline{T}$		
	1	t	D	0
	2	f	D	−6
IX		J		
	1	t	W	0
	2	f	W	−6
X		X		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XI		$\overline{S}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XII		F		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XIII		R		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
XIV		H		
	1	t	C	0
	2	f	C	−6
XV		$\overline{M}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

198. Matrix Card Assembly 548332

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, K, L, S, U, $\overline{H}$, J, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{C}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8. Connect load 2 in series between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set the corresponding LOAD switch to position 8.

e. Insert matrix assembly 548332 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{K}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
II		$\overline{U}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
III		U		
	1	t	V	0
	2	f	V	−6
IV		E		
	1	t	W	0
	2	f	W	−6
V		K		
	1	t	D	0
	2	f	D	−6
VI		S		
	1	t	C	0
	2	f	C	−6
VII		$\overline{H}$ $\overline{P}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		$\overline{H}$ $\overline{R}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{P}$ $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
X		$\overline{R}$ $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XI		K L $\overline{J}$ $\overline{S}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

199. Matrix Card Assembly 548334

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, H, L, M, R, S, T, V, X, Y, Z, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{D}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548334 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		M Y Z		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
II		M T Y		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
III		R S Y $\overline{M}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IV		Y Z $\overline{M}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
V		T Y $\overline{M}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VI		M R S Y		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VII		$\overline{U}$		
	1	t	$\overline{C}$, $\overline{W}$	0
	2	f	$\overline{C}$, $\overline{W}$	−6
VIII		H $\overline{H}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		E $\overline{N}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		E V		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		L J $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		$\overline{L}$ $\overline{S}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		X		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

200. Matrix Card Assembly 548336

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, U, V, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{D}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 switch to position 8.

e. Insert matrix assembly 548336 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{P}$ $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
II		Y $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
III		F $\overline{B}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IV		H S V $\overline{B}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		M R $\overline{A}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VI		W X		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		J N Z		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		S Z $\overline{B}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		V Z $\overline{B}$ $\overline{V}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		L P $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XI		L Z $\overline{B}$ $\overline{F}$ $\overline{H}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XII		K L $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		K U $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIV		P $\overline{E}$ $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

201. Matrix Card Assembly 548338

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, P, T, U, V, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Connect LOAD 1 in series between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 switch to position 8.

d. Press SELECT switch 1 on.

e. Insert matrix assembly 548338 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H $\overline{F}$ $\overline{S}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		$\overline{F}$ $\overline{M}$ $\overline{P}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		Y $\overline{F}$ $\overline{M}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IV		W $\overline{B}$ $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
V		F X		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VI		L M P W		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		W $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		J V $\overline{V}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		$\overline{M}$ $\overline{T}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		J T U $\overline{P}$ $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XI		J K T $\overline{P}$ $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XII		$\overline{N}$ $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		K T W $\overline{B}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XIV		K T Z $\overline{B}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XV		W $\overline{A}$ $\overline{K}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XVI		V $\overline{A}$ $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks $\overline{E}$ and $\overline{Y}$.

l. Remove the matrix assembly from the test jack.

202. Matrix Card Assembly 548340

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, S, T, W, Y, Z, $\overline{A}$, $\overline{D}$, $\overline{F}$, J, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 switch to position 8.

e. Insert matrix assembly 548340 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L Z $\overline{R}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		J $\overline{D}$ $\overline{S}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		J K L $\overline{D}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IV		J S W $\overline{D}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
V		J $\overline{D}$ $\overline{P}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VI		J S Z $\overline{D}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VII		J T V		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VIII		H K $\overline{A}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IX		E K $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
X		N $\overline{J}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XI		L $\overline{J}$ $\overline{K}$ $\overline{N}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		S W J $\overline{K}$ $\overline{U}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIII		F $\overline{L}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XIV		D M $\overline{A}$ $\overline{N}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XV		E W $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

203. Matrix Card Assembly 548343

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, K, L, M, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD 1 switch to position 8.

e. Insert matrix assembly 548343 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L M P R		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		L M R $\overline{F}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
III		L M W $\overline{A}$ $\overline{V}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
IV		L M P $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
V		H R S T U		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VI		H K W $\overline{D}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VII		H $\overline{D}$ $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VIII		F K $\overline{R}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IX		H S $\overline{D}$ $\overline{K}$ $\overline{P}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
X		K W $\overline{R}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XI		L W Y $\overline{D}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		K Z $\overline{B}$ $\overline{H}$ $\overline{V}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
XIII		X Y $\overline{C}$ $\overline{M}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove the matrix assembly from the test jack.

j. Return all TRUE-FALSE switches to neutral positions.

204. Matrix Card Assembly 548344

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, E, F, H, J, M, N, P, R, S, T, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks V and DC VOLTAGES −50 with jumper leads, and set LOAD 1 switch to position 8.

e. Insert matrix assembly 548344 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J N		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
II		Z $\overline{A}$ $\overline{T}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
III		T $\overline{A}$ $\overline{T}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
IV		M R S $\overline{A}$ $\overline{T}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		M R S $\overline{L}$ T		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
VI		C		
	1	t	W	0
	2	f	W	−6
VII		T		
	1	t	W	0
	2	f	W	−6
VIII		R S $\overline{B}$ $\overline{K}$ T		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
IX		R S $\overline{M}$ T		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		T $\overline{B}$ T		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XI		Z $\overline{B}$ T		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		F H		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIII		E $\overline{F}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		P Y		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks U and $\overline{Y}$, and jacks $\overline{E}$ and $\overline{Y}$.

l. Remove the matrix assembly from the test jack.

205. Matrix Card Assembly 548347

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, L, M, N, P, R, S, T, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548347 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E P $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		F H S $\overline{B}$ $\overline{T}$		
	1	t t t t t	D	0
	2	f t t t t	D	−6
	3	t f t t t	D	−6
	4	t t f t t	D	−6
	5	t t t f t	D	−6
	6	t t t t f	D	−6
III		E H $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IV		P S $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
V		$\overline{K}$ $\overline{T}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		S $\overline{A}$ $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VII		S $\overline{M}$ $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VIII		$\overline{L}$ $\overline{T}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IX		N T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
X		M T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		Z $\overline{C}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		R $\overline{J}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		$\overline{J}$ $\overline{P}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		L N		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XV		Y $\overline{J}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVI		J X		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and K; $\overline{Y}$ and U; and $\overline{Y}$ and $\overline{F}$.

j. Remove the matrix assembly from the test jack.

206. Matrix Card Assembly 548348

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, R, U, W, X, Y, Z, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks C and DC VOLTAGES −50 with jumper leads, and set LOAD 1 switch to position 8.

e. Insert matrix assembly 548348 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{F}$ $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		H W		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
III		F $\overline{B}$ $\overline{U}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		L $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
V		H Z		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		K $\overline{K}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		N U $\overline{D}$ $\overline{T}$ $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		K $\overline{E}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		R $\overline{D}$ $\overline{T}$ $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		M $\overline{D}$ $\overline{E}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		U $\overline{D}$ $\overline{P}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XII		Y $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIII		J N $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		J K		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XV		K $\overline{M}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVI		X		
	1	t	V	0
	2	f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks $\overline{Y}$ and T.

l. Remove the matrix assembly from the test jack.

207. Matrix Card Assembly 548350

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, R, T, U, V, X, Y, $\overline{F}$, J, $\overline{K}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks C and DC VOLTAGES −50 with jumper leads and set LOAD 1 switch to position 8.

e. Insert matrix assembly 548350 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L $\overline{K}$ $\overline{P}$ T $\overline{U}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
II		L V $\overline{T}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		D F H $\overline{V}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		J R U $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		J M $\overline{U}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VI		E F		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		E R		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VIII		V X $\overline{T}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		M N $\overline{T}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
X		M $\overline{J}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XI		$\overline{J}$ $\overline{S}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XII		K T		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XIII		V $\overline{J}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XIV		N T V		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XV		N T Y		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XVI		E V $\overline{F}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

208. Matrix Card Assembly 548352

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, F, J, K, L, M, P, R, S, U, V, W, X, Y, Z, $\overline{A}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{D}$ and DC VOLTAGES −50 with jumper leads, and set LOAD 1 switch to position 8.

e. Insert matrix assembly 548352 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F P		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		L U $\overline{S}$ $\overline{T}$ $\overline{U}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
III		K L U $\overline{T}$ $\overline{U}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		L R $\overline{E}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		L M U $\overline{T}$ $\overline{U}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
VI		D $\overline{A}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		L $\overline{R}$ $\overline{V}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		J L $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		J Z $\overline{N}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
X		V $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		S U $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		W $\overline{C}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		Y $\overline{J}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIV		X		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XV		Y $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Measure 10,000 ohms between jacks $\overline{K}$ and $\overline{Y}$.

l. Remove the matrix assembly from the test jack.

209. Matrix Card Assembly 548354

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, H, J, K, L, M, N, P, R, S, X, Y, Z, $\overline{A}$, B, $\overline{F}$, $\overline{H}$, J, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD 1 in series between jacks $\overline{W}$ and DC VOLTAGES −28 with jumper leads, and set LOAD switch to position 8.

e. Insert matrix assembly 548354 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N $\overline{A}$ $\overline{L}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		K L $\overline{A}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		K $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IV		M $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
V		$\overline{N}$ $\overline{P}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VI		Z $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VII		H S Y $\overline{F}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VIII		Z $\overline{F}$ $\overline{M}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		N $\overline{B}$ $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
X		E N $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XI		M $\overline{F}$ $\overline{J}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XII		P $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		X $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIV		J $\overline{H}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XV		R $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XVI		Y $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

210. Matrix Card Assembly 548356

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548356 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		M N P		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		R T		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
III		H L Z $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IV		L M N		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
V		E F J L		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VI		X Z		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VII		L R $\overline{B}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VIII		L $\overline{B}$ $\overline{P}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IX		K L R $\overline{J}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
X		D S U Y $\overline{A}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
XI		N $\overline{A}$ $\overline{M}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XII		H K $\overline{F}$ $\overline{H}$ $\overline{U}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIII		$\overline{A}$ L $\overline{S}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

211. Matrix Card Assembly 548358

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, L, P, R, S, U, W, Z, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548358 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P R $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		P R S		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		W H $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		E F L U $\overline{F}$ $\overline{K}$ $\overline{R}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
V		J		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VI		Z		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VII		$\overline{S}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VIII		J		
	1	t	V	0
	2	f	V	−6
IX		Z		
	1	t	V	0
	2	f	V	−6
X		$\overline{S}$		
	1	t	V	0
	2	f	V	−6
XI		H		
	1	t	D	0
	2	f	D	−6
XII		$\overline{E}$ J $\overline{V}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIII		S J $\overline{V}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		W $\overline{H}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XV		E F L U $\overline{F}$ $\overline{R}$ $\overline{T}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
XVI		H		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

212. Matrix Card Assembly 548360

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, K, R, S, T, U, Z, $\overline{E}$, $\overline{H}$, J, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548360 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S T Z $\overline{S}$ $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
II		T Z $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		K Z J $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		F S Z $\overline{S}$ $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		S T Z $\overline{E}$ J		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		K T Z $\overline{E}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VII		S Z $\overline{E}$ $\overline{H}$ J		
	1	t t t t t	V	0
	2	f t t t t	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		E R $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		K Z $\overline{E}$ $\overline{H}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
X		U		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XI		U		
	1	t	C	0
	2	f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

213. Matrix Card Assembly 548362

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches J, K, L, N, P, R, S, T, U, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, J, $\overline{K}$, $\overline{L}$, $\overline{N}$, and $\overline{P}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548362 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P R $\overline{K}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
II		N $\overline{P}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
III		K $\overline{P}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IV		K N		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
V		L		
	1	t	V, W	0
	2	f	V, W	−6
VI		S Z		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		T $\overline{A}$ $\overline{L}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		S U $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{E}$ $\overline{F}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
X		J		
	1	t	X	0
	2	f	X	−6
XI		$\overline{J}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

214. Matrix Card Assembly 548364

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, J, K, N, P, R, S, $\overline{K}$, $\overline{P}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548364 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P R S $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
II		E N R $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
III		E P R $\overline{K}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		N R S $\overline{K}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		E K P $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VI		K N S $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		K P S $\overline{K}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		E K N $\overline{K}$		
	1	t t t t	$\overline{D}$	−6
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		J		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
X		$\overline{T}$		
	1	t	W	0
	2	f	W	−6
XI		$\overline{T}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

215. Matrix Card Assembly 548366

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, J, N, P, R, S, X, $\overline{A}$, E, F, H, J, K, P, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks V and DC VOLTAGES −50 with jumper leads, and set LOAD 1 switch to position 8.

e. Insert matrix assembly 548366 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{A}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
II		$\overline{F}$ J $\overline{P}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
III		$\overline{F}$ $\overline{K}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		P $\overline{E}$ $\overline{F}$ $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		N $\overline{E}$ $\overline{F}$ $\overline{K}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VI		$\overline{P}$ $\overline{S}$ $\overline{T}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		J $\overline{K}$ $\overline{T}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		N $\overline{E}$ $\overline{P}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		P $\overline{E}$ $\overline{K}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		E X $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		R S $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		S X $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		$\overline{A}$		
	1	t	V	0
	2	f	V	−6
XIV		J		
	1	t	V	0
	2	f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

216. Matrix Card Assembly 548368

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches C, E, H, J, K, N, P, R, S, T, U, X, $\overline{E}$, $\overline{H}$, $\overline{K}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548368 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J P R T $\overline{N}$ $\overline{V}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
II		J N P U $\overline{N}$ $\overline{V}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
III		H $\overline{H}$ $\overline{K}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		K $\overline{K}$ $\overline{R}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		H S $\overline{E}$ $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		K X $\overline{E}$ $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		H $\overline{R}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		K $\overline{H}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		H X $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		K S $\overline{E}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		C		
	1	t	D	0
	2	f	D	−6
XII		E		
	1	t	F	0
	2	f	F	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

217. Matrix Card Assembly 548370

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, K, L, S, T, Z, $\overline{E}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, P, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548370 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
II		S		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		S T Z $\overline{S}$ $\overline{T}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IV		K T $\overline{J}$ $\overline{T}$[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		F K $\overline{E}$ J[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		F S $\overline{E}$ $\overline{S}$[a]		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VII		$\overline{K}$ $\overline{L}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		$\overline{M}$ $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		$\overline{H}$ $\overline{T}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
X		$\overline{E}$ $\overline{R}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		L		
	1	t	V	0
	2	f	V	−6
XII		$\overline{L}$ $\overline{P}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIII		$\overline{K}$ $\overline{M}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6

[a] Set TRUE-FALSE switch Z to TRUE for tests IV, V, and VI.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

218. Matrix Card Assembly 548372

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, H, J, K, L, N, P, R, S, T, X, Y, $\overline{E}$, $\overline{H}$, J, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548372 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K $\overline{H}$ $\overline{T}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		H X $\overline{E}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		H $\overline{R}$ $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		K S $\overline{E}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		L		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		E $\overline{N}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VII		R $\overline{N}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		J $\overline{K}$ T		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
IX		N $\overline{E}$ $\overline{P}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
X		$\overline{P}$ $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6
XI		P $\overline{E}$ $\overline{K}$		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6
XII		L		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
XIII		Y $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XIV		Y $\overline{E}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XV		T Y $\overline{T}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XVI		J Y		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

219. Matrix Card Assembly 548392

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches B, F, H, J, P, R, S, T, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548392 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R S Z		
	1	t t t	D	0
	2	t t f	D	−6
II		R S $\overline{T}$		
	1	t t t	D	0
	2	t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		R S $\overline{H}$		
	1	t t t	D	0
	2	t t f	D	−6
IV		R S $\overline{U}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		$\overline{A}$ $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VI		$\overline{M}$		
	1	t	V	0
	2	f	V	−6
VII		Z $\overline{K}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VIII		$\overline{K}$ $\overline{N}$ $\overline{T}$		
	1	t t t	$\overline{W}$	0
	2	t t f	$\overline{W}$	−6
IX		$\overline{K}$ $\overline{N}$ $\overline{U}$		
	1	t t t	$\overline{W}$	0
	2	t t f	$\overline{W}$	−6
X		$\overline{H}$ $\overline{K}$ $\overline{N}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XI		F $\overline{L}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		$\overline{M}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XIII		B		
	1	t	C	0
	2	f	C	−6
XIV		H		
	1	t	E	0
	2	f	E	−6
XV		P		
	1	t	U	0
	2	f	U	−6
XVI		J		
	1	t	W	0
	2	f	W	−6
XVII		T		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XVIII		$\overline{F}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
XIX		$\overline{J}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

220. Matrix Card Assembly 548394

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, K, L, M, N, P, R, S, T, U, Z, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548394 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P R $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		K P $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		P T $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		P Z $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		J $\overline{P}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		F M U $\overline{J}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		M U $\overline{H}$ $\overline{J}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		N U $\overline{K}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		F M $\overline{E}$ $\overline{J}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		M $\overline{E}$ $\overline{H}$ J		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		N $\overline{E}$ $\overline{F}$ $\overline{N}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XII		J $\overline{L}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIII		L S $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		S $\overline{E}$ $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XV		S U $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

221. Matrix Card Assembly 548396

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, J, K, P, R, S, U, X, Z, $\overline{B}$, $\overline{C}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks V and DC VOLTAGES −50 with jumper leads, and set LOAD 1 switch to position 8.

e. Insert matrix assembly 548396 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J $\overline{T}$ $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		F J $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		J $\overline{F}$ J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		S X $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		S $\overline{H}$ $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		J P		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VII		P $\overline{T}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VIII		P $\overline{C}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IX		R $\overline{M}$ $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
X		K $\overline{M}$ $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XI		F P		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		Z $\overline{B}$ $\overline{M}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XIII		Z $\overline{K}$ $\overline{M}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XIV		P $\overline{P}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

222. Matrix Card Assembly 548398

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, E, F, H, J, K, L, M, N, P, R, S, T, U, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548398 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H N P $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
II		H N P $\overline{N}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		J P $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		J P $\overline{J}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		J P $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		F P $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		E P $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		P $\overline{E}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		R S $\overline{A}$ $\overline{L}$ $\overline{M}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
X		$\overline{B}$ $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		C $\overline{H}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		K S T		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIII		K L U $\overline{A}$ $\overline{S}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XIV		K M U $\overline{A}$ $\overline{F}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

223. Matrix Card Assembly 548400

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches C, E, J, K, L, N, P, R, S, T, U, X, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{C}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548400 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		T $\overline{A}$ $\overline{H}$ $\overline{U}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t t	$\overline{C}$ $\overline{C}$	−6
	4	t t f t	$\overline{C}$ $\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
II		P T $\overline{H}$ $\overline{U}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t t	$\overline{C}$ $\overline{C}$	−6
	4	t t f t	$\overline{C}$ $\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		S $\overline{A}$ $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$ $\overline{C}$	−6
	3	t f t	$\overline{C}$ $\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		P S $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		R $\overline{A}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VI		$\overline{A}$ $\overline{E}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VII		E $\overline{A}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		Z $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		L $\overline{A}$ $\overline{J}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		J X $\overline{A}$ $\overline{L}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XI		N X $\overline{L}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XII		L $\overline{T}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIII		C L		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIV		K U		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

224. Matrix Card Assembly 548402

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, N, P, R, S, $\overline{A}$, $\overline{B}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548402 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P $\overline{A}$ $\overline{B}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		P R S $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		H R $\overline{A}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		H S $\overline{B}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		F J $\overline{L}$ $\overline{S}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		J $\overline{K}$ $\overline{N}$ $\overline{S}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VII		$\overline{K}$ $\overline{L}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VIII		F $\overline{N}$ $\overline{S}$ $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IX		$\overline{H}$ $\overline{L}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
X		$\overline{A}$ $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and $\overline{E}$ and $\overline{Y}$ and N.

j. Remove the matrix assembly from the test jack.

225. Matrix Card Assembly 548404

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, N, P, R, T, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548404 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		X $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		$\overline{E}$ $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
III		F $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		E $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		P Y $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		J $\overline{N}$ $\overline{S}$ $\overline{U}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VII		H N $\overline{L}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VIII		R $\overline{M}$ $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		T $\overline{A}$ $\overline{M}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		Z $\overline{A}$ $\overline{B}$ $\overline{M}$ $\overline{R}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XI		Z $\overline{A}$ $\overline{F}$ $\overline{K}$ $\overline{M}$ $\overline{R}$		
	1	t t t t t t	$\overline{C}$	0
	2	f t t t t t	$\overline{C}$	−6
	3	t f t t t t	$\overline{C}$	−6
	4	t t f t t t	$\overline{C}$	−6
	5	t t t f t t	$\overline{C}$	−6
	6	t t t t f t	$\overline{C}$	−6
	7	t t t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

226. Matrix Card Assembly 548406

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, J, K, L, T, U, X, Y, $\overline{A}$, $\overline{F}$, $\overline{H}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 in series between jacks $\overline{C}$ and DC VOLTAGES −50 with jumper lead, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548406 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{N}$ $\overline{P}$ $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
II		K X $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		K T $\overline{N}$ $\overline{U}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IV		$\overline{F}$ $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		J $\overline{N}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		$\overline{M}$		
	1	t	C	0
	2	f	C	−6
VII		$\overline{H}$ $\overline{N}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		U $\overline{N}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		E $\overline{N}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
X		L $\overline{A}$ $\overline{N}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XI		Y $\overline{N}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

227. Matrix Card Assembly 548409

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, L, N, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{M}$, $\overline{N}$, P, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548409 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{M}$ $\overline{P}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		$\overline{H}$ $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
III		E $\overline{M}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IV		P $\overline{M}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
V		T U		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
VI		F $\overline{N}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		$\overline{M}$		
	1	t	V	0
	2	f	V	−6
VIII		L N $\overline{N}$		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6
IX		F L Y		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6
X		H L Z		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		L $\overline{R}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6
XII		$\overline{B}$		
	1	t	X	0
	2	f	X	−6
XIII		$\overline{A}$ $\overline{S}$ $\overline{T}$		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6
XIV		$\overline{M}$		
	1	t	X	0
	2	f	X	−6
XV		$\overline{J}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XVI		R		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
XVII		$\overline{F}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XVIII		S		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to the neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and H, $\overline{Y}$ and R, and $\overline{Y}$ and J.

j. Remove the matrix assembly from the test jack.

228. Matrix Card Assembly 548411

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches H, J, L, N, P, T, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548411 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N $\overline{A}$ $\overline{D}$ $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		N $\overline{A}$ $\overline{D}$ $\overline{F}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		N $\overline{A}$ $\overline{D}$ $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		X Z $\overline{B}$ $\overline{D}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		H		
	1	t	V	0
	2	f	V	−6
VI		$\overline{M}$		
	1	t	V	0
	2	f	V	−6
VII		N $\overline{R}$ $\overline{W}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		L $\overline{N}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		J T Y $\overline{H}$ J $\overline{K}$ $\overline{L}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
X		$\overline{C}$		
	1	t	W	0
	2	f	W	−6
XI		P		
	1	t	U	0
	2	f	U	−6
XII		$\overline{P}$		
	1	t	D	0
	2	f	D	−6
XIII		$\overline{T}$		
	1	t	C	0
	2	f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to the neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and E; $\overline{Y}$ and F; $\overline{Y}$ and K; $\overline{Y}$ and M; $\overline{Y}$ and P; $\overline{Y}$ and $\overline{C}$; $\overline{Y}$ $\overline{Y}$ and $\overline{F}$; $\overline{Y}$ and $\overline{P}$; $\overline{Y}$ and $\overline{S}$; $\overline{Y}$ and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

229. Matrix Card Assembly 548413

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, M, Y, $\overline{F}$, $\overline{H}$, $\overline{K}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548413 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F M Y		
	1	t t t	$\overline{N}$	0
	2	f t t	$\overline{N}$	−6
	3	t f t	$\overline{N}$	−6
	4	t t f	$\overline{N}$	−6
II		K		
	1	t	C	0
	2	f	C	−6
III		K		
	1	t	D	0
	2	f	D	−6
IV		F		
	1	t	E	0
	2	f	E	−6
V		$\overline{H}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		$\overline{R}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VII		$\overline{S}$		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
VIII		H		
	1	t	L	0
	2	f	L	−6
IX		$\overline{F}$		
	1	t	V	0
	2	f	V	−6
X		$\overline{S}$		
	1	t	W	0
	2	f	W	−6
XI		J		
	1	t	X	0
	2	f	X	−6
XII		F		
	1	t	U	0
	2	f	U	−6
XIII		$\overline{R}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XIV		H		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XV		J		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and P; $\overline{Y}$ and R; $\overline{Y}$ and S; $\overline{Y}$ and T; $\overline{Y}$ and $\overline{H}$; $\overline{Y}$ and $\overline{K}$; $\overline{Y}$ and $\overline{M}$; $\overline{Y}$ and $\overline{P}$; $\overline{Y}$ and $\overline{T}$; and $\overline{Y}$ and J.

j. Remove the matrix assembly from the test jack.

230. Matrix Card Assembly 548415

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, H, J, L, P, S, T, X, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548415 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J P		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
II		E J		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		H P		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		E H		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
V		L $\overline{E}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VI		$\overline{P}$ $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VII		$\overline{K}$ $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		$\overline{L}$ $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		$\overline{M}$ $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
X		L $\overline{H}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		X		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XII		S		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XIII		T		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XIV		Y		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XV		Z		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XVI		$\overline{A}$		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6
XVII		P $\overline{N}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XVIII		E $\overline{N}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

231. Matrix Card Assembly 548417

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, M, N, P, R, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548417 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		M $\overline{M}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		M $\overline{L}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
III		M $\overline{S}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
IV		M $\overline{N}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		M $\overline{U}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VI		M $\overline{B}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		P R		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VIII		E R		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		$\overline{P}$ $\overline{U}$		
	1	t t	L	0
	2	f t	L	−6
	3	t f	L	−6
X		N $\overline{K}$		
	1	t t	L	0
	2	f t	L	−6
	3	t f	L	−6
XI		$\overline{K}$ $\overline{P}$		
	1	t t	J	0
	2	f t	J	−6
	3	t f	J	−6
XII		N $\overline{U}$		
	1	t t	J	0
	2	f t	J	−6
	3	t f	J	−6
XIII		X		
	1	t	F	0
	2	f	F	−6
XIV		S		
	1	t	F	0
	2	f	F	−6
XV		T		
	1	t	F	0
	2	f	F	−6
XVI		Y		
	1	t	F	0
	2	f	F	−6
XVII		Z		
	1	t	F	0
	2	f	F	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVIII		$\overline{A}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

232. Matrix Card Assembly 548419

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, R, T, U, X, Y, Z, $\overline{B}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548419 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
II		H		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
III		J		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
IV		K		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
V		$\overline{P}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
VI		$\overline{R}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
VII		$\overline{S}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
VIII		M T		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IX		M N		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
X		M Z		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		M X		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		L R X Z $\overline{B}$ $\overline{L}$ $\overline{N}$		
	1	t t t t t t t	$\overline{U}$	0
	2	f t t t t t t	$\overline{U}$	−6
	3	t f t t t t t	$\overline{U}$	−6
	4	t t f t t t t	$\overline{U}$	−6
	5	t t t f t t t	$\overline{U}$	−6
	6	t t t t f t t	$\overline{U}$	−6
	7	t t t t t f t	$\overline{U}$	−6
	8	t t t t t t f	$\overline{U}$	−6
XIII		M Y		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		M U		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XV		L M		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XVI		M R		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and P; $\overline{Y}$ and $\overline{F}$; and $\overline{Y}$ and $\overline{R}$.

j. Remove the matrix assembly from the test jack.

233. Matrix Card Assembly 548421

Note. The schematic diagram is in TM 11-5840-271-30/20

a. Set TRUE-FALSE switches E, F, L, N, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548421 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F Y $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		Y $\overline{S}$ $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		R Y $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		F S Y $\overline{J}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		P T Z $\overline{K}$ $\overline{R}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VI		E L Z $\overline{K}$ $\overline{R}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VII		U $\overline{B}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		L P Z $\overline{P}$ $\overline{R}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
IX		E T Z $\overline{P}$ $\overline{R}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
X		E L N $\overline{A}$ $\overline{B}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XI		N P T $\overline{A}$ $\overline{B}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XII		P Z $\overline{B}$ $\overline{E}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

234. Matrix Card Assembly 548423

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a load in series between jack $\overline{D}$ and DC VOLTAGES −50 with jumper leads, and set LOAD switch to position 8.

e. Insert matrix assembly 548423 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Y $\overline{J}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
II		S $\overline{B}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
III		K X $\overline{B}$ $\overline{F}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		E Z $\overline{P}$ $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		N P $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		P Z $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		R $\underline{L}$ $\overline{N}$ T		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		F J P $\overline{B}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		H Y		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		P $\overline{R}$ $\overline{S}$ $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XI		E $\overline{H}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XII		F		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIII		L $\overline{H}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

235. Matrix Card Assembly 548425

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, K, L, P, R, S, Y, $\overline{E}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548425 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E $\overline{H}$ J $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		P $\overline{H}$ $\overline{P}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		E $\overline{P}$ $\overline{R}$ $\overline{S}$ $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IV		P $\overline{J}$ $\overline{R}$ $\overline{S}$ $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		Y		
	1	t	V	0
	2	f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		E H		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		L H J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		L P U		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		K R K L R V		
	1	t t t t t t	W	0
	2	f t t t t t	W	−6
	3	t f t t t t	W	−6
	4	t t f t t t	W	−6
	5	t t t f t t	W	−6
	6	t t t t f t	W	−6
	7	t t t t t f	W	−6
X		S R M		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XI		Y M		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XII		F M		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

236. Matrix Card Assembly 548427

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, K, L, N, P, R, S, X, Y, B, E, F, H, J, K, L, M, N, P, R, S, T, and U to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548427 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H P M R		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
II		P S K R		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
III		Y H J		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IV		R Y H		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		E F Y S		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		F Y $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		L Y		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		S $\overline{B}$ $\overline{E}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		S $\overline{B}$ $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
X		N S $\overline{B}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XI		K X $\overline{B}$ $\overline{F}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		S $\overline{P}$ $\overline{U}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XIII		H $\overline{N}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIV		N		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

237. Matrix Card Assembly 548429

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, H, N, R, S, Y, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a load in series between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set LOAD switch to position 8.

e. Insert matrix assembly 548429 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{L}$ $\overline{P}$ $\overline{R}$ $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		H Y		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		R Y		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IV		Y $\overline{S}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		S Y $\overline{J}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		N $\overline{B}$ $\overline{M}$ $\overline{U}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VII		N $\overline{B}$ $\overline{F}$ $\overline{K}$ $\overline{M}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		E Y $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		$\overline{B}$ $\overline{D}$ $\overline{E}$ $\overline{K}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		$\overline{F}$ $\overline{H}$ $\overline{K}$ $\overline{L}$ $\overline{R}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XI		$\overline{K}$ $\overline{L}$ $\overline{P}$ $\overline{R}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XII		$\overline{H}$ $\overline{L}$ $\overline{R}$ $\overline{U}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XIII		$\overline{F}$ $\overline{L}$ $\overline{P}$ $\overline{R}$ $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

238. Matrix Card Assembly 548431

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, L, N, P, R, S, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548431 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the

sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N $\overline{K}$ $\overline{M}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		$\overline{H}$ K $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		R $\overline{S}$ $\overline{T}$ $\overline{V}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		P S $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		F S $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		F H $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		H P $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		U Y		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IX		X $\overline{B}$ $\overline{F}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
X		Z $\overline{E}$ $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XI		J Y $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		L $\overline{B}$ $\overline{W}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		L $\overline{B}$ $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

239. Matrix Card Assembly 548432

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, J, K, L, N, R, S, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{H}$, $\overline{K}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548432 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H K $\overline{K}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		K $\overline{K}$ $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		K S Z		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		H K Z		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		$\overline{A}$		
	1	t	W	0
	2	f	W	−6
VI		N $\overline{E}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		E $\overline{E}$ $\overline{H}$ $\overline{R}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VIII		F L Y $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IX		J R Y $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
X		$\overline{A}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

240. Matrix Card Assembly 548438

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, P, R, S, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{L}$, $\overline{M}$, and $\overline{P}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548438 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F $\overline{B}$ $\overline{M}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		$\overline{P}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
III		P $\overline{B}$ $\overline{E}$ $\overline{M}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		P $\overline{L}$ $\overline{M}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
V		P S $\overline{B}$ F $\overline{H}$ J $\overline{L}$		
	1	t t t t t t t	C	0
	2	f t t t t t t	C	−6
	3	t f t t t t t	C	−6
	4	t t f t t t t	C	−6
	5	t t t f t t t	C	−6
	6	t t t t f t t	C	−6
	7	t t t t t f t	C	−6
	8	t t t t t t f	C	−6
VI		P R S $\overline{B}$ $\overline{H}$ J $\overline{L}$		
	1	t t t t t t t	C	0
	2	f t t t t t t	C	−6
	3	t f t t t t t	C	−6
	4	t t f t t t t	C	−6
	5	t t t f t t t	C	−6
	6	t t t t f t t	C	−6
	7	t t t t t f t	C	−6
	8	t t t t t t f	C	−6
VII		F		
	1	t	V	0
	2	f	V	−6
VIII		H J Z		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IX		$\overline{A}$		
	1	t	D	0
	2	f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

241. Matrix Card Assembly 548440

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, N, P, R, S, T, U, X, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548440 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K $\overline{F}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		K $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		K R U		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		F K U		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		E Z $\overline{S}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
VI		J $\overline{E}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		H $\overline{E}$ F $\overline{S}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VIII		$\overline{A}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		$\overline{A}$		
	1	t	W	0
	2	f	W	−6
X		N P $\overline{S}$		
	1	t t t	B	0
	2	f t t	B	−6
	3	t f t	B	−6
	4	t t f	B	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		S T X		
	1	t t t	Y	0
	2	f t t	Y	−6
	3	t f t	Y	−6
	4	t t f	Y	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

242. Matrix Card Assembly 548445

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, N, P, R, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548445 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L $\overline{L}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
II		H $\overline{M}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		U $\overline{L}$ $\overline{R}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		E $\overline{H}$ $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		Y $\overline{L}$ $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		K $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		$\overline{B}$ $\overline{L}$ $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		Z J $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		$\overline{F}$ $\overline{K}$ $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		P $\overline{M}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		$\overline{E}$ $\overline{L}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XII		F $\overline{A}$ $\overline{L}$ $\overline{T}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XIII		J N $\overline{A}$ $\overline{L}$ $\overline{P}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XIV		X		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XV		R		
	1	t	$\overline{X}$	0
	2	f	$\overline{X}$	−6
XVI		D		
	1	t	B	0
	2	f	B	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to the neutral positions.

i. Measure 33,000 ohms between jacks M and $\overline{V}$.

j. Remove the matrix assembly from the test jack.

243. Matrix Card Assembly 548447

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches K, N, P, U, $\overline{F}$, J, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548447 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N $\overline{P}$ $\overline{S}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
II		N J $\overline{K}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
III		$\overline{F}$ $\overline{K}$ $\overline{P}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IV		$\overline{F}$ J $\overline{S}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		N J $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		N $\overline{K}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	6
	3	t f t	V	−6
	4	t t f	V	−6
VII		$\overline{F}$ J $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		P $\overline{M}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
IX		U $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
X		K $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	6
XI		$\overline{N}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XII		$\overline{K}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XIII		$\overline{S}$		
	1	t	E	0
	2	f	E	−6
XIV		$\overline{F}$ $\overline{P}$ $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

244. Matrix Card Assembly 548449

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, P, R, S, Y, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, and $\overline{L}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548449 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K Y $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		P $\overline{E}$ J $\overline{L}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		H $\overline{E}$ $\overline{F}$ $\overline{L}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		S $\overline{A}$ $\overline{F}$ $\overline{H}$ $\overline{L}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		F S $\overline{A}$ $\overline{L}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		F J $\overline{A}$ $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VII		R Y $\overline{L}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VIII		D E		
	1	t t	N	0
	2	f t	N	−6
	3	t f	N	−6
IX		L $\overline{F}$		
	1	t t	N	0
	2	f t	N	−6
	3	t f	N	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

245. Matrix Card Assembly 548451

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, P, R, S, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548451 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K $\overline{L}$ $\overline{N}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
II		P $\overline{E}$ J $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
III		H $\overline{E}$ $\overline{F}$ $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IV		S $\overline{A}$ $\overline{F}$ $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
V		$\overline{A}$ $\overline{F}$ $\overline{H}$ $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		R $\overline{L}$ $\overline{N}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		H J $\overline{E}$ $\overline{L}$ $\overline{P}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VIII		$\overline{A}$ $\overline{L}$ $\overline{P}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		F $\overline{A}$ $\overline{L}$ $\overline{P}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
X		E F		
	1	t t	N	0
	2	f t	N	−6
	3	t f	N	−6
XI		L S		
	1	t t	N	0
	2	f t	N	−6
	3	t f	N	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

246. Matrix Card Assembly 548453

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, K, L, N, P, R, X, Y, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548453 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E N $\overline{K}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		N $\overline{K}$ $\overline{R}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		$\overline{F}$ $\overline{S}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IV		$\overline{U}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
V		K L Y		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		L P X J		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		H L X $\overline{H}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VIII		L R Y		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		K L $\overline{N}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
X		L P X J		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
XI		H L X $\overline{H}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
XII		L R $\overline{N}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		F H L X $\overline{T}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XIV		$\overline{N}$		
	1	t	C	0
	2	f	C	−6
XV		R $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

247. Matrix Card Assembly 548455

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, N, P, R, S, T, U, Y, Z, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548455 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E U		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
II		F N $\overline{H}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
III		H $\overline{F}$ $\overline{H}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IV		J N Y		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
V		K Y $\overline{F}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		N P $\overline{N}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VII		R $\overline{P}$ $\overline{N}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VIII		N S $\overline{B}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IX		T $\overline{B}$ $\overline{F}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
X		N Z $\overline{P}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XI		Z $\overline{F}$ $\overline{R}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XII		N $\overline{K}$ $\overline{S}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XIII		$\overline{F}$ $\overline{K}$ $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

248. Matrix Card Assembly 548457

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches M, R, S, T, U, V, W, X, Y, Z, $\overline{B}$, $\overline{H}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548457 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R U		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		S $\overline{H}$ $\overline{M}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		T $\overline{H}$ $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		M S Y		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
V		V Y $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VI		S W $\overline{N}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VII		S $\overline{B}$ $\overline{P}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VIII		$\overline{B}$ $\overline{L}$ $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IX		S Z $\overline{S}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
X		Z $\overline{L}$ $\overline{T}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XI		X $\overline{L}$ $\overline{N}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

249. Matrix Card Assembly 548459

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, T, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks C and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548459 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P S $\overline{K}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		R $\overline{K}$ $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		S $\overline{C}$ $\overline{M}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		T $\overline{C}$ $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
V		S $\overline{D}$ $\overline{P}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VI		$\overline{D}$ $\overline{L}$ $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VII		S $\overline{E}$ $\overline{S}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VIII		$\overline{E}$ $\overline{L}$ T		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IX		J K		
	1	t t	$\overline{B}$	0
	2	f t	$\overline{B}$	−6
	3	t f	$\overline{B}$	−6
X		L M N		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6
XI		F H		
	1	t t	$\overline{B}$	0
	2	f t	$\overline{B}$	−6
	3	t f	$\overline{B}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

250. Matrix Card Assembly 548460

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, F, H, J, K, L, M, S, T, Y, Z, F, $\overline{H}$, J, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548460 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F J Z $\overline{\text{N}}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		F $\overline{\text{F}}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
III		$\overline{\text{R}}$		
	1	t	D	0
	2	f	D	−6
IV		H K J		
	1	t t t	E	0
	2	f t t	E	−6
	3	t f t	E	−6
	4	t t f	E	−6
V		F H T $\overline{\text{H}}$ $\overline{\text{K}}$ $\overline{\text{N}}$		
	1	t t t t t t	$\overline{\text{D}}$	0
	2	f t t t t t	$\overline{\text{D}}$	−6
	3	t f t t t t	$\overline{\text{D}}$	−6
	4	t t f t t t	$\overline{\text{D}}$	−6
	5	t t t f t t	$\overline{\text{D}}$	−6
	6	t t t t f t	$\overline{\text{D}}$	−6
	7	t t t t t f	$\overline{\text{D}}$	−6
VI		Y		
	1	t	$\overline{\text{E}}$	0
	2	f	$\overline{\text{E}}$	−6
VII		F H T $\overline{\text{H}}$ J $\overline{\text{K}}$		
	1	t t t t t t	$\overline{\text{C}}$	0
	2	f t t t t t	$\overline{\text{C}}$	−6
	3	t f t t t t	$\overline{\text{C}}$	−6
	4	t t f t t t	$\overline{\text{C}}$	−6
	5	t t t f t t	$\overline{\text{C}}$	−6
	6	t t t t f t	$\overline{\text{C}}$	−6
	7	t t t t t f	$\overline{\text{C}}$	−6
VIII		F L Z		
	1	t t t	$\overline{\text{B}}$	0
	2	f t t	$\overline{\text{B}}$	−6
	3	t f t	$\overline{\text{B}}$	−6
	4	t t f	$\overline{\text{B}}$	−6
IX		B M Z		
	1	t t t	$\overline{\text{B}}$	0
	2	f t t	$\overline{\text{B}}$	−6
	3	t f t	$\overline{\text{B}}$	−6
	4	t t f	$\overline{\text{B}}$	−6
X		H J $\overline{\text{S}}$		
	1	t t t	$\overline{\text{V}}$	0
	2	f t t	$\overline{\text{V}}$	−6
	3	t f t	$\overline{\text{V}}$	−6
	4	t t f	$\overline{\text{V}}$	−6
XI		H $\overline{\text{N}}$ $\overline{\text{S}}$		
	1	t t t	$\overline{\text{W}}$	0
	2	f t t	$\overline{\text{W}}$	−6
	3	t f t	$\overline{\text{W}}$	−6
	4	t t f	$\overline{\text{W}}$	−6
XII		S		
	1	t	$\overline{\text{U}}$	0
	2	f	$\overline{\text{U}}$	−6
XIII		H J $\overline{\text{P}}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		H $\overline{\text{N}}$ $\overline{\text{P}}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XV		H K $\overline{N}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Remove the matrix assembly from the test jack.

251. Matrix Card Assembly 548464

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, P, S, T, U, V, W, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548464 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
II		L $\overline{L}$ $\overline{P}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		F M $\overline{B}$ $\overline{K}$ $\overline{N}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
IV		F M W $\overline{N}$ $\overline{T}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
V		L $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		J $\overline{N}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VII		N $\overline{H}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		P Z		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		D P		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		J L U $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		K N T		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		N S $\overline{L}$ $\overline{S}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XIII		$\overline{L}$ $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIV		H V $\overline{E}$ $\overline{F}$ $\overline{L}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
XV		H $\overline{F}$ $\overline{L}$ $\overline{S}$ $\overline{U}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

252. Matrix Card Assembly 548466

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, S, T, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548466 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K T Y $\overline{A}$ $\overline{D}$ $\overline{F}$ $\overline{L}$ $\overline{U}$		
	1	t t t t t t t t	V	0
	2	f t t t t t t t	V	−6
	3	t f t t t t t t	V	−6
	4	t t f t t t t t	V	−6
	5	t t t f t t t t	V	−6
	6	t t t t f t t t	V	−6
	7	t t t t t f t t	V	−6
	8	t t t t t t f t	V	−6
	9	t t t t t t t f	V	−6
II		F J N $\overline{B}$ $\overline{H}$ $\overline{T}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
III		F J N W $\overline{H}$ $\overline{K}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
IV		$\overline{R}$		
	1	t	V	0
	2	f	V	−6
V		$\overline{B}$ J		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		W J		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		L $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		E X $\overline{L}$ $\overline{P}$ $\overline{S}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IX		H $\overline{L}$ $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		L W		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		S $\overline{J}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
XII		Z		
	1	t	R	0
	2	f	R	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

253. Matrix Card Assembly 548468

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches B, C, D, E, F, H, J, K, L, M, N, P, R, S, T, U, W, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548468 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{S}$[a]		
	1	t	V	0
	2	f	V	−6
II		F P $\overline{A}$ $\overline{C}$ $\overline{F}$ $\overline{U}$[a]		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
III		H $\overline{N}$ $\overline{P}$ $\overline{R}$[a]		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		B $\overline{N}$[a]		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		F J P U $\overline{U}$[a]		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		$\overline{M}$ L $\overline{N}$[a]		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		T $\overline{M}$ $\overline{V}$[a]		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		E F K P $\overline{U}$[a]		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IX		C D L N R Z $\overline{E}$ J[a]		
	1	t t t t t t t t	V	0
	2	f t t t t t t t	V	−6
	3	t f t t t t t t	V	−6
	4	t t f t t t t t	V	−6
	5	t t t f t t t t	V	−6
	6	t t t t f t t t	V	−6
	7	t t t t t f t t	V	−6
	8	t t t t t t f t	V	−6
	9	t t t t t t t f	V	−6
X		B $\overline{Z}$[a]		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		$\overline{B}$[b]		
	1	t	V	0
	2	f	V	−6
XII		$\overline{W}$[b]		
	1	t	V	0
	2	f	V	−6

[a] Set TRUE-FALSE switch W to TRUE.

[b] Set TRUE-FALSE switch S to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

254. Matrix Card Assembly 548470

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Set TRUE-FALSE switches C, D, E, F, H, J, K, L, M, N, P, R, S, T, U, V, W, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548470 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		D $\overline{P}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		D E		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
III		W Z		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IV		F		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
V		P X		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		T X $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		J K X		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		C L N R S X $\overline{E}$ J		
	1	t t t t t t t t	$\overline{D}$	0
	2	f t t t t t t t	$\overline{D}$	−6
	3	t f t t t t t t	$\overline{D}$	−6
	4	t t f t t t t t	$\overline{D}$	−6
	5	t t t f t t t t	$\overline{D}$	−6
	6	t t t t f t t t	$\overline{D}$	−6
	7	t t t t t f t t	$\overline{D}$	−6
	8	t t t t t t f t	$\overline{D}$	−6
	9	t t t t t t t f	$\overline{D}$	−6
IX		M P		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		$\overline{H}$ $\overline{N}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		H M Y $\overline{F}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XII		P V		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIII		$\overline{S}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
XIV		H X $\overline{B}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XV		C U X $\overline{L}$ $\overline{M}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

255. Matrix Card Assembly 548472

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, L, M, N, P, S, T, U, Y, Z, $\overline{A}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548472 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		S Y $\overline{N}$ $\overline{R}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
III		S Y $\overline{M}$ $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IV		N S Y $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
V		D P S		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VI		N T $\overline{D}$ $\overline{E}$ $\overline{V}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VII		P S Z $\overline{F}$ $\overline{L}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VIII		M S $\overline{T}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		L P S $\overline{E}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
X		H S T U $\overline{H}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
XI		S T $\overline{L}$ $\overline{S}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		L T $\overline{P}$ $\overline{X}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XIII		S $\overline{A}$ $\overline{K}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
XIV		F J P S		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XV		F P S $\overline{J}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

256. Matrix Card Assembly 548474

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, M, N, P, R, S, T, U, W, $\overline{C}$, F, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548474 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P S $\overline{M}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		R $\overline{N}$ $\overline{V}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		R J $\overline{R}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		F J N T		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		L T J $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		T $\overline{C}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		H T $\overline{V}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VIII		D T $\overline{U}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IX		N T $\overline{P}$ $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
X		N T $\overline{S}$ $\overline{V}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XI		K T $\overline{V}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XII		T J $\overline{L}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	4	t t f t	C	−6
	5	t t t f	C	−6
XIII		T $\overline{L}$ $\overline{P}$ $\overline{V}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XIV		E		
	1	t	V	0
	2	f	V	−6
XV		U $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVI		M W $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

257. Matrix Card Assembly 548476

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, N, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks C and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548476 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K P S $\overline{M}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		J N P S		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		R S $\overline{N}$ $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		L R $\overline{R}$ $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		K R S $\overline{M}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		F Y $\overline{H}$ $\overline{L}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		L $\overline{A}$ J $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VIII		F L T $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IX		L T $\overline{S}$ $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
X		H T U J		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XI		H L R $\overline{H}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XII		T $\overline{H}$ $\overline{N}$ $\overline{S}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XIII		E		
	1	t	W	0
	2	f	W	−6
XIV		Z F $\overline{K}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

258. Matrix Card Assembly 548478

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, F, H, J, K, L, M, N, P, R, S, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548478 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F $\overline{J}$ $\overline{L}$ $\overline{T}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		J R $\overline{S}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		R J $\overline{L}$ $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
IV		R $\overline{H}$ L $\overline{U}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		F N $\overline{J}$ $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
VI		D F $\overline{J}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VII		N P R S $\overline{E}$ $\overline{J}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
VIII		H L $\overline{C}$ $\overline{M}$ $\overline{R}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
IX		H K M $\overline{M}$ $\overline{R}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
X		$\overline{A}$ $\overline{K}$ $\overline{V}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XI		R $\overline{N}$ $\overline{S}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
XII		H Z $\overline{B}$ $\overline{D}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
XIII		H $\overline{F}$ $\overline{M}$ $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

259. Matrix Card Assembly 548480

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, L, M, N, P, R, S, T, U, W, Y, $\overline{E}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548480 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N P $\overline{H}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	3	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		D P $\overline{H}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		F P $\overline{H}$ $\overline{L}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IV		N R $\overline{H}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
V		F L Y $\overline{J}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VI		F L Y $\overline{K}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VII		J L Y $\overline{H}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VIII		Y $\overline{H}$ $\overline{M}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IX		Y $\overline{H}$ $\overline{L}$ $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
X		H L S T W $\overline{E}$ $\overline{J}$		
	1	t t t t t t t	$\overline{W}$	0
	2	f t t t t t t	$\overline{W}$	−6
	3	t f t t t t t	$\overline{W}$	−6
	4	t t f t t t t	$\overline{W}$	−6
	5	t t t f t t t	$\overline{W}$	−6
	6	t t t t f t t	$\overline{W}$	−6
	7	t t t t t f t	$\overline{W}$	−6
	8	t t t t t t f	$\overline{W}$	−6
XI		M $\overline{K}$ $\overline{L}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		M $\overline{L}$ $\overline{S}$ $\overline{X}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches				Test point	Output voltage
XIII		E	M	U	$\overline{X}$		
	1	t	t	t	t	$\overline{W}$	0
	2	f	t	t	t	$\overline{W}$	−6
	3	t	f	t	t	$\overline{W}$	−6
	4	t	t	f	t	$\overline{W}$	−6
	5	t	t	t	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

260. Matrix Card Assembly 548482

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, L, N, R, S, T, U, V, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548482 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
I		H	L	S	T	W	$\overline{E}$	$\overline{K}$		
	1	t	t	t	t	t	t	t	$\overline{W}$	0
	2	f	t	t	t	t	t	t	$\overline{W}$	−6
	3	t	f	t	t	t	t	t	$\overline{W}$	−6
	4	t	t	f	t	t	t	t	$\overline{W}$	−6
	5	t	t	t	f	t	t	t	$\overline{W}$	−6
	6	t	t	t	t	f	t	t	$\overline{W}$	−6
	7	t	t	t	t	t	f	t	$\overline{W}$	−6
	8	t	t	t	t	t	t	f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches					Test point	Output voltage
II		K	R	$\overline{U}$				
	1	t	t	t			$\overline{W}$	0
	2	f	t	t			$\overline{W}$	−6
	3	t	f	t			$\overline{W}$	−6
	4	t	t	f			$\overline{W}$	−6
III		J	N	$\overline{A}$	$\overline{H}$			
	1	t	t	t	t		$\overline{W}$	0
	2	f	t	t	t		$\overline{W}$	−6
	3	t	f	t	t		$\overline{W}$	−6
	4	t	t	f	t		$\overline{W}$	−6
	5	t	t	t	f		$\overline{W}$	−6
IV		L	$\overline{A}$	$\overline{P}$	$\overline{U}$			
	1	t	t	t	t		$\overline{W}$	0
	2	f	t	t	t		$\overline{W}$	−6
	3	t	f	t	t		$\overline{W}$	−6
	4	t	t	f	t		$\overline{W}$	−6
	5	t	t	t	f		$\overline{W}$	−6
V		R	Z	$\overline{M}$	$\overline{U}$			
	1	t	t	t	t		$\overline{W}$	0
	2	f	t	t	t		$\overline{W}$	−6
	3	t	f	t	t		$\overline{W}$	−6
	4	t	t	f	t		$\overline{W}$	−6
	5	t	t	t	f		$\overline{W}$	−6
VI		N	R	S	$\overline{E}$	$\overline{U}$		
	1	t	t	t	t	t	$\overline{W}$	0
	2	f	t	t	t	t	$\overline{W}$	−6
	3	t	f	t	t	t	$\overline{W}$	−6
	4	t	t	f	t	t	$\overline{W}$	−6
	5	t	t	t	f	t	$\overline{W}$	−6
	6	t	t	t	t	f	$\overline{W}$	−6
VII		R	$\overline{B}$					
	1	t	t				$\overline{W}$	0
	2	f	t				$\overline{W}$	−6
	3	t	f				$\overline{W}$	−6
VIII		D	$\overline{D}$					
	1	t	t				$\overline{C}$	0
	2	f	t				$\overline{C}$	−6
	3	t	f				$\overline{C}$	−6
IX		E						
	1	t					$\overline{C}$	0
	2	f					$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		V X $\overline{F}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XI		U X $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		F L Y $\overline{H}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XIII		H L S T W $\overline{E}$ $\overline{H}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

261. Matrix Card Assembly 548484

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches C, D, E, F, J, K, N, P, R, U, W, X, Y, Z, $\overline{A}$, $\overline{C}$, $\overline{E}$, F, $\overline{H}$, J, K, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks $\overline{D}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548484 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J R $\overline{E}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
II		J P $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		J N X		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		C J K $\overline{A}$ F $\overline{N}$		
	1	t t t t t t	$\overline{D}$	0
	2	f t t t t t	$\overline{D}$	−6
	3	t f t t t t	$\overline{D}$	−6
	4	t t f t t t	$\overline{D}$	−6
	5	t t t f t t	$\overline{D}$	−6
	6	t t t t f t	$\overline{D}$	−6
	7	t t t t t f	$\overline{D}$	−6
V		J W $\overline{R}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		J $\overline{C}$ F $\overline{N}$ $\overline{T}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VII		E W $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		J $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
IX		E X P $\overline{R}$ $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
X		C E J		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XI		C E U		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		E F Y		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		D Z $\overline{C}$ $\overline{V}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XIV		D Y $\overline{C}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XV		C D $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

262. Matrix Card Assembly 548486

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, J, K, L, M, N, P, R, S, T, U, W, X, Z, $\overline{A}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548486 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R T $\overline{E}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		K T $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		D T $\overline{A}$ $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IV		F T		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		N S T $\overline{C}$ $\overline{F}$ $\overline{U}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
VI		P S T $\overline{H}$ $\overline{N}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VII		P T X $\overline{A}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		E J X		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		E $\overline{C}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		E Z $\overline{C}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		E $\overline{H}$ $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		E U $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		E U $\overline{C}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIV		D W Z		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XV		J L $\overline{H}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVI		M		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

263. Matrix Card Assembly 548488

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, D, E, F, H, J, K, M, N, P, R, S, T, U, W, X, Y, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, J, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8. Connect LOAD 2 between jacks L and DC VOLTAGES −50 with jumper leads, and set the corresponding LOAD selector switch to position 8.

e. Insert matrix assembly 548488 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E R $\overline{E}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		E P W		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		E S X		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		D E N $\overline{F}$ $\overline{N}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		E F N T $\overline{T}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		E $\overline{A}$ $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		E K S $\overline{M}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		E $\overline{M}$ $\overline{P}$ $\overline{R}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		K M R S		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		J D J		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		F U Y		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		F K U V		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XIII		C H M W E		
	1	t t t t t	L	0
	2	f t t t t	L	−6
	3	t f t t t	L	−6
	4	t t f t t	L	−6
	5	t t t f t	L	−6
	6	t t t t f	L	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

264. Matrix Card Assembly 548490

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, K, L, N, P, R, U, V, W, X, Y, Z, A, B, E, H, J, P, R, S, T, and V to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks C and DC VOLTAGES, −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548490 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R E T		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		D S T		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		F Y T		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		P A B T		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
V		R T		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		D E Z		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		D E Y $\overline{V}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VIII		E F $\overline{R}$ $\overline{V}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IX		D U $\overline{J}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		D U $\overline{R}$ $\overline{V}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XI		F U J $\overline{V}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	C	−6
XII		F N U		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIII		H U $\overline{B}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIV		V X $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XV		K L W		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

265. Matrix Card Assembly 548492

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, F, H, J, K, L, M, N, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{M}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548492 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J K W $\overline{C}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		D $\overline{A}$ $\overline{R}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		D Z $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		F N $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		M $\overline{A}$ $\overline{H}$ $\overline{T}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		D T $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		Y $\overline{A}$ $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VIII		$\overline{A}$ $\overline{B}$ $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		$\overline{A}$ J $\overline{M}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		P		
	1	t	V	0
	2	f	V	−6
XI		U X $\overline{D}$ $\overline{S}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XII		H L R X $\overline{S}$ $\overline{U}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
XIII		R S X $\overline{E}$ $\overline{S}$ $\overline{U}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

266. Matrix Card Assembly 548494

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches B, C, D, E, F, H, J, P, T, U, W, X, Y, $\overline{B}$, $\overline{D}$, $\overline{F}$, $\overline{H}$, J, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, $\overline{W}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks $\overline{N}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548494 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		D U $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		U $\overline{B}$ $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		J U $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IV		D X $\overline{S}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		P		
	1	t	V	0
	2	f	V	−6
VI		E J $\overline{M}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		T X $\overline{B}$ $\overline{R}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		H Y $\overline{D}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		$\overline{B}$ $\overline{L}$ $\overline{P}$ $\overline{R}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
X		F W $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		B C W		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		U $\overline{M}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIII		P		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIV		J U $\overline{B}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XV		Y $\overline{R}$ $\overline{V}$ $\overline{W}$		
	1	t t t t	$\overline{N}$	0
	2	f t t t	$\overline{N}$	−6
	3	t f t t	$\overline{N}$	−6
	4	t t f t	$\overline{N}$	−6
	5	t t t f	$\overline{N}$	−6
XVI		H U W $\overline{T}$ $\overline{V}$ $\overline{W}$ X		
	1	t t t t t t t	$\overline{N}$	0
	2	f t t t t t t	$\overline{N}$	−6
	3	t f t t t t t	$\overline{N}$	−6
	4	t t f t t t t	$\overline{N}$	−6
	5	t t t f t t t	$\overline{N}$	−6
	6	t t t t f t t	$\overline{N}$	−6
	7	t t t t t f t	$\overline{N}$	−6
	8	t t t t t t f	$\overline{N}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

267. Matrix Card Assembly 548496

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, J, K, L, R, S, T, W, X, Y, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks V and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548496 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		C J T W		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
II		C J W $\overline{J}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		C J S W $\overline{F}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IV		L R X $\overline{R}$ $\overline{U}$ $\overline{V}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6
V		R X $\overline{K}$ $\overline{R}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		K Y $\overline{B}$ $\overline{J}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		R X $\overline{L}$ $\overline{R}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		$\overline{A}$ $\overline{H}$ $\overline{P}$ $\overline{S}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IX		$\overline{H}$ $\overline{M}$ $\overline{N}$ $\overline{P}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
X		K S Y $\overline{B}$ $\overline{F}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

268. Matrix Card Assembly 548498

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, K, M, N, P, V, Y, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{M}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect LOAD 1 between jacks $\overline{W}$ and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548498 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Y $\overline{F}$ $\overline{M}$ $\overline{R}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		D E Y $\overline{C}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
III		P Y $\overline{E}$ $\overline{M}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
IV		K N Y $\overline{M}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
V		M $\overline{H}$ $\overline{J}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		M $\overline{A}$ $\overline{B}$ $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VII		D M V $\overline{P}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

269. Matrix Card Assembly 548502

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, H, J, K, L, M, N, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548502 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		L $\overline{T}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
II		R J $\overline{T}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		M $\overline{L}$ $\overline{U}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		$\overline{L}$ $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
V		D $\overline{M}$ $\overline{W}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		D $\overline{K}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		E		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
VIII		J $\overline{E}$ $\overline{H}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		X		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
X		$\overline{N}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
XI		K	N	S	U	Y	Z	$\overline{B}$		
	1	t	t	t	t	t	t	t	$\overline{C}$	0
	2	f	t	t	t	t	t	t	$\overline{C}$	−6
	3	t	f	t	t	t	t	t	$\overline{C}$	−6
	4	t	t	f	t	t	t	t	$\overline{C}$	−6
	5	t	t	t	f	t	t	t	$\overline{C}$	−6
	6	t	t	t	t	f	t	t	$\overline{C}$	−6
	7	t	t	t	t	t	f	t	$\overline{C}$	−6
	8	t	t	t	t	t	t	f	$\overline{C}$	−6
XII		P	T							
	1	t	t						V	0
	2	f	t						V	−6
	3	t	f						V	−6
XIII		P	$\overline{V}$							
	1	t	t						V	0
	2	f	t						V	−6
	3	t	f						V	−6
XIV		J	W	$\overline{A}$	F					
	1	t	t	t	t				V	0
	2	f	t	t	t				V	−6
	3	t	f	t	t				V	−6
	4	t	t	f	t				V	−6
	5	t	t	t	f				V	−6
XV		E								
	1	t							V	0
	2	f							V	−6
XVI		X								
	1	t							V	0
	2	f							V	−6
XVII		H	P							
	1	t	t						V	0
	2	f	t						V	−6
	3	t	f						V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

270. Matrix Card Assembly 548504

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches C, E, F, K, M, N, R, S, T, U, V, X, Y, Z, $\overline{A}$, B, $\overline{D}$, $\overline{E}$, J, $\overline{M}$, $\overline{N}$, P, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548504 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches					Test point	Output voltage
I		T	$\overline{E}$	$\overline{N}$				
	1	t	t	t			W	0
	2	f	t	t			W	−6
	3	t	f	t			W	−6
	4	t	t	f			W	−6
II		T	$\overline{E}$	$\overline{W}$				
	1	t	t	t			W	0
	2	f	t	t			W	−6
	3	t	f	t			W	−6
	4	t	t	f			W	−6
III		T	V	$\overline{E}$				
	1	t	t	t			W	0
	2	f	t	t			W	−6
	3	t	f	t			W	−6
	4	t	t	f			W	−6
IV		N	J	$\overline{M}$	T	$\overline{V}$		
	1	t	t	t	t	t	W	0
	2	f	t	t	t	t	W	−6
	3	t	f	t	t	t	W	−6
	4	t	t	f	t	t	W	−6
	5	t	t	t	f	t	W	−6
	6	t	t	t	t	f	W	−6
V		F						
	1	t					W	0
	2	f					W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		X		
	1	t	W	0
	2	f	W	−6
VII		K S U Y $\overline{A}$ $\overline{B}$ $\overline{S}$		
	1	t t t t t t t	W	0
	2	f t t t t t t	W	−6
	3	t f t t t t t	W	−6
	4	t t f t t t t	W	−6
	5	t t t f t t t	W	−6
	6	t t t t f t t	W	−6
	7	t t t t t f t	W	−6
	8	t t t t t t f	W	−6
VIII		F		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		C $\overline{D}$ $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		C $\overline{D}$ $\overline{W}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XI		C V $\overline{D}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XII		K M S U Z $\overline{B}$ $\overline{S}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
XIII		X		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIV		N $\overline{M}$ $\overline{R}$ $\overline{V}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XV		R		
	1	t	P	0
	2	f	P	−6
XVI		E		
	1	t	D	0
	2	f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

271. Matrix Card Assembly 548506

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches C, D, E, F, H, J, K, L, N, P, R, S, T, U, V, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{S}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548506 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
II		E N T $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
III		E N $\overline{L}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IV		D H J L W $\overline{K}$ $\overline{M}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t f t t t t t	$\overline{D}$	−6
	4	t t f t t t t	$\overline{D}$	−6
	5	t t t f t t t	$\overline{D}$	−6
	6	t t t t f t t	$\overline{D}$	−6
	7	t t t t t f t	$\overline{D}$	−6
	8	t t t t t t f	$\overline{D}$	−6
V		E N V $\overline{L}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VI		D L R W $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VII		C $\overline{A}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		F		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IX		X		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
X		K S U Y Z $\overline{B}$ $\overline{S}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t f t t t t t	$\overline{D}$	−6
	4	t t f t t t t	$\overline{D}$	−6
	5	t t t f t t t	$\overline{D}$	−6
	6	t t t t f t t	$\overline{D}$	−6
	7	t t t t t f t	$\overline{D}$	−6
	8	t t t t t t f	$\overline{D}$	−6
XI		D H L P W J $\overline{M}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t f t t t t t	$\overline{D}$	−6
	4	t t f t t t t	$\overline{D}$	−6
	5	t t t f t t t	$\overline{D}$	−6
	6	t t t t f t t	$\overline{D}$	−6
	7	t t t t t f t	$\overline{D}$	−6
	8	t t t t t t f	$\overline{D}$	−6
XII		E $\overline{H}$ $\overline{L}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

272. Matrix Card Assembly 548508

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, K, M, N, P, S, T, U, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{S}$, $\overline{T}$, $\overline{V}$, $\overline{W}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.
c. Press SELECT switch 1 on.
d. Insert matrix assembly 548508 into test jack J1.
e. Press the ENERGIZE switch on.
f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		D E $\overline{L}$ $\overline{W}$		
	1	t t t t		0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
II		D E $\overline{K}$ $\overline{L}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
III		D E $\overline{P}$ $\overline{W}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IV		X		
	1	t	W	0
	2	f	W	−6
V		$\overline{N}$		
	1	t	W	0
	2	f	W	−6
VI		$\overline{N}$		
	1	t	W	0
	2	f	W	−6
VII		F		
	1	t	W	0
	2	f	W	−6
VIII		K N S U Y $\overline{A}$ $\overline{B}$		
	1	t t t t t t t	W	0
	2	f t t t t t t	W	−6
	3	t f t t t t t	W	−6
	4	t t f t t t t	W	−6
	5	t t t f t t t	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	6	t t t t f t t	W	−6
	7	t t t t t f t	W	−6
	8	t t t t t t f	W	−6
IX		P $\overline{E}$ H		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
X		J Z $\overline{C}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XI		M T $\overline{A}$ $\overline{B}$ F J $\overline{M}$ $\overline{S}$ $\overline{T}$ $\overline{X}$		
	1	t t t t t t t t t t	C	0
	2	f t t t t t t t t t	C	−6
	3	t f t t t t t t t t	C	−6
	4	t t f t t t t t t t	C	−6
	5	t t t f t t t t t t	C	−6
	6	t t t t f t t t t t	C	−6
	7	t t t t t f t t t t	C	−6
	8	t t t t t t f t t t	C	−6
	9	t t t t t t t f t t	C	−6
	10	t t t t t t t t f t	C	−6
	11	t t t t t t t t t f	C	−6
XII		H M T $\overline{A}$ $\overline{B}$ J $\overline{S}$ $\overline{X}$		
	1	t t t t t t t t	V	0
	2	f t t t t t t t	V	−6
	3	t f t t t t t t	V	−6
	4	t t f t t t t t	V	−6
	5	t t t f t t t t	V	−6
	6	t t t t f t t t	V	−6
	7	t t t t t f t t	V	−6
	8	t t t t t t f t	V	−6
	9	t t t t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

273. Matrix Card Assembly 548510

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches B, C, D, H, J, K, M, N, P, R, S, T, Z, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548510 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H N $\overline{X}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
II		$\overline{F}$		
	1	t	U	0
	2	f	U	−6
III		$\overline{F}$		
	1	t	W	0
	2	f	W	−6
IV		K		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
V		D S $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		$\overline{E}$ $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VII		J Z $\overline{M}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VIII		P R $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		M P $\overline{R}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		C $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		P J $\overline{N}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		$\overline{D}$		
	1	t	V	0
	2	f	V	−6
XIII		$\overline{R}$ $\overline{S}$ $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIV		B J $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XV		T J T $\overline{U}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XVI		$\overline{B}$ $\overline{U}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVII		R $\overline{K}$ $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVIII		$\overline{F}$		
	1	t	$\overline{A}$	0
	2	f	$\overline{A}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

274. Matrix Card Assembly 548512

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches B, C, H, J, L, M, N, T, W, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{H}$, $\overline{K}$, $\overline{M}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548512 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H J L W		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		C J		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
III		$\overline{U}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IV		M		
	1	t	S	0
	2	f	S	−6
V		$\overline{M}$		
	1	t	S	0
	2	f	S	−6
VI		$\overline{H}$		
	1	t	S	0
	2	f	S	−6
VII		Z		
	1	t	S	0
	2	f	S	−6
VIII		N		
	1	t	S	0
	2	f	S	−6
IX		$\overline{K}$		
	1	t	S	0
	2	f	S	−6
X		Y		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XI		$\overline{M}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XII		$\overline{H}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XIII		$\overline{A}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		N		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XV		$\overline{K}$		
	1	t	$\overline{F}$	0
	2	f	$\overline{F}$	−6
XVI		M N $\overline{A}$ $\overline{B}$ $\overline{K}$ $\overline{T}$		
	1	t t t t t t	$\overline{N}$	0
	2	f t t t t t	$\overline{N}$	−6
	3	t f t t t t	$\overline{N}$	−6
	4	t t f t t t	$\overline{N}$	−6
	5	t t t f t t	$\overline{N}$	−6
	6	t t t t f t	$\overline{N}$	−6
	7	t t t t t f	$\overline{N}$	−6
XVII		T		
	1	t	V	0
	2	f	V	−6
XVIII		B		
	1	t	D	0
	2	f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{L}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

275. Matrix Card Assembly 548514

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, M, N, P, R, S, Z, $\overline{A}$, $\overline{H}$, J, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548514 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{H}$		
	1	t	J	0
	2	f	J	−6
II		$\overline{A}$		
	1	t	J	0
	2	f	J	−6
III		$\overline{S}$		
	1	t	J	0
	2	f	J	−6
IV		$\overline{K}$		
	1	t	J	0
	2	f	J	−6
V		M		
	1	t	J	0
	2	f	J	−6
VI		$\overline{M}$		
	1	t	J	0
	2	f	J	−6
VII		$\overline{H}$		
	1	t	K	0
	2	f	K	−6
VIII		Z		
	1	t	K	0
	2	f	K	−6
IX		$\overline{S}$		
	1	t	K	0
	2	f	K	−6
X		$\overline{K}$		
	1	t	K	0
	2	f	K	−6
XI		M		
	1	t	K	0
	2	f	K	−6
XII		$\overline{M}$		
	1	t	K	0
	2	f	K	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIII		$\overline{H}$		
	1	t	L	0
	2	f	L	−6
XIV		$\overline{A}$		
	1	t	L	0
	2	f	L	−6
XV		N		
	1	t	L	0
	2	f	L	−6
XVI		$\overline{K}$		
	1	t	L	0
	2	f	L	−6
XVII		M		
	1	t	L	0
	2	f	L	−6
XVIII		$\overline{M}$		
	1	t	L	0
	2	f	L	−6
XIX		H		
	1	t	C	0
	2	f	C	−6
XX		S		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
XXI		$\overline{T}$		
	1	t	E	0
	2	f	E	−6
XXII		J		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
XXIII		F		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XXIV		$\overline{P}$		
	1	t	D	0
	2	f	D	−6
XXV		P		
	1	t	B	0
	2	f	B	−6
XXVI		R		
	1	t	T	0
	2	f	T	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

276. Matrix Card Assembly 548516

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, P, R, $\overline{F}$, J, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548516 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches				Test point	Output voltage
I		P	R	$\overline{F}$	J		
	1	t	t	t	t	C	0
	2	f	t	t	t	C	−6
	3	t	f	t	t	C	−6
	4	t	t	f	t	C	−6
	5	t	t	t	f	C	−6
II		F	R	J	$\overline{T}$		
	1	t	t	t	t	U	0
	2	f	t	t	t	U	−6
	3	t	f	t	t	U	−6
	4	t	t	f	t	U	−6
	5	t	t	t	f	U	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		H P $\overline{F}$ J		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
IV		F H $\overline{F}$ J		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		H P J $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		F H J $\overline{T}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VII		P R $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		F R $\overline{F}$ $\overline{S}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IX		P R $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
X		F H $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{U}$	0
	2	f t t t	$\overline{U}$	−6
	3	t f t t	$\overline{U}$	−6
	4	t t f t	$\overline{U}$	−6
	5	t t t f	$\overline{U}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

277. Matrix Card Assembly 548518

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, N, P, R, S, T, U, X, Y, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548518 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R S J $\overline{K}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		K U F H K		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
III		J S Y F H K		
	1	t t t t t t	E	0
	2	f t t t t t	E	−6
	3	t f t t t t	E	−6
	4	t t f t t t	E	−6
	5	t t t f t t	E	−6
	6	t t t t f t	E	−6
	7	t t t t t f	E	−6
IV		S U Y H K U		
	1	t t t t t t	E	0
	2	f t t t t t	E	−6
	3	t f t t t t	E	−6
	4	t t f t t t	E	−6
	5	t t t f t t	E	−6
	6	t t t t f t	E	−6
	7	t t t t t f	E	−6
V		S U X F K R		
	1	t t t t t t	$\overline{E}$	0
	2	f t t t t t	$\overline{E}$	−6
	3	t f t t t t	$\overline{E}$	−6
	4	t t f t t t	$\overline{E}$	−6
	5	t t t f t t	$\overline{E}$	−6
	6	t t t t f t	$\overline{E}$	−6
	7	t t t t t f	$\overline{E}$	−6
VI		J S X H K U		
	1	t t t t t t	$\overline{E}$	0
	2	f t t t t t	$\overline{E}$	−6
	3	t f t t t t	$\overline{E}$	−6
	4	t t f t t t	$\overline{E}$	−6
	5	t t t f t t	$\overline{E}$	−6
	6	t t t t f t	$\overline{E}$	−6
	7	t t t t t f	$\overline{E}$	−6
VII		T U F H P		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VIII		F N S T		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IX		H P L S		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
X		F H L S		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
XI		H P S T		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

278. Matrix Card Assembly 548520

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, N, P, R, S, T, X, Y, Z, $\overline{F}$, J, $\overline{L}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548520 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Y Z		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		F J $\overline{J}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		F J R		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		F S $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		F H S		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VI		K L $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VII		F J X		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
VIII		K $\overline{L}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		N $\overline{J}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		N R		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		L T $\overline{J}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		N S X		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		T $\overline{J}$ $\overline{L}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XIV		P $\overline{F}$		
	1	t t	$\overline{P}$	0
	2	f t	$\overline{P}$	−6
	3	t f	$\overline{P}$	−6
XV		P $\overline{U}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6

g. Press the ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 33,000 ohms between jacks M and jacks C, D, V, and $\overline{V}$.

j. Connect positive lead of ohmmeter to jack C and negative lead to jack $\overline{S}$, and measure 100 ohms maximum. Reverse meter leads and measure 100,000 ohms minimum.

k. Remove the matrix assembly from the test jack.

279. Matrix Card Assembly 548522

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches H, J, K, L, S, T, Y, Z, J, $\overline{K}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548522 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		Y Z		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
II		T		
	1	t	E	0
	2	f	E	−6
III		K		
	1	t	W	0
	2	f	W	−6
IV		$\overline{K}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
V		$\overline{P}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VI		S $\overline{K}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		J $\overline{K}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		S $\overline{J}$ $\overline{K}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
IX		S $\overline{K}$ $\overline{R}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
X		L		
	1	t	F	0
	2	f	F	−6
XI		H S $\overline{J}$ $\overline{K}$		
	1	t t t t	U	0
	2	f t t t	U	−6
	3	t f t t	U	−6
	4	t t f t	U	−6
	5	t t t f	U	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 33,000 ohms between jacks M and jacks D, X, $\overline{B}$, and $\overline{C}$.

j. Remove the matrix assembly from the test jack.

280. Matrix Card Assembly 548524

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, L, P, R, U, $\overline{B}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548524 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P		
	1	t	C	0
	2	f	C	−6
II		F $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		F $\overline{L}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
IV		P R J		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
V		F $\overline{B}$ $\overline{T}$		
	1	t t t	$\overline{E}$	0
	2	f t t	$\overline{E}$	−6
	3	t f t	$\overline{E}$	−6
	4	t t f	$\overline{E}$	−6
VI		F R $\overline{B}$ $\overline{T}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		F H $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VIII		F H J $\overline{T}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IX		F H $\overline{S}$ $\overline{T}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		L U $\overline{F}$		
	1	t t t	E	0
	2	f t t	E	−6
	3	t f t	E	−6
	4	t t f	E	−6
XI		J L $\overline{F}$		
	1	t t t	T	0
	2	f t t	T	−6
	3	t f t	T	−6
	4	t t f	T	−6
XII		L U $\overline{F}$ $\overline{H}$		
	1	t t t t	$\overline{U}$	0
	2	f t t t	$\overline{U}$	−6
	3	t f t t	$\overline{U}$	−6
	4	t t f t	$\overline{U}$	−6
	5	t t t f	$\overline{U}$	−6
XIII		L U $\overline{F}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 3,300 ohms between jack M and jacks X and $\overline{N}$.

j. Remove the matrix assembly from the test jack.

281. Matrix Card Assembly 548526

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, L, M, P, R, S, T, U, W, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{M}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548526 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E R T $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		M J $\overline{M}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
III		Z		
	1	t	C	0
	2	f	C	−6
IV		H P $\overline{F}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
V		F U Y $\overline{F}$ $\overline{H}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
VI		Z		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
VII		S U $\overline{B}$ $\overline{F}$ $\overline{H}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
VIII		S U W $\overline{F}$ $\overline{R}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
IX		F H $\overline{F}$ $\overline{H}$ $\overline{K}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
X		H S X $\overline{F}$ $\overline{H}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XI		H S $\overline{E}$ $\overline{F}$ $\overline{R}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
XII		$\overline{L}$ $\overline{U}$ $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

282. Matrix Card Assembly 548528

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, P, R, T, U, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{H}$, and $\overline{J}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548528 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K R $\overline{E}$ $\overline{H}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		F $\overline{E}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
III		E $\overline{J}$		
	1	t t	$\overline{T}$	0
	2	f t	$\overline{T}$	−6
	3	t f	$\overline{T}$	−6
IV		P		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
V		J Z $\overline{B}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VI		J U $\overline{B}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VII		J T $\overline{A}$ $\overline{B}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VIII		H Z $\overline{B}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
IX		J U $\overline{B}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
X		H $\overline{A}$ $\overline{B}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Measure 5,100 ohms between jacks M and $\overline{V}$.

i. Return all TRUE-FALSE switches to neutral positions.

j. Remove the matrix assembly from the test jack.

283. Matrix Card Assembly 548530

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, K, M, P, R, S, T, W, X, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548530 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K X		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	W	−6
II		E $\overline{L}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	W	−6
III		T X		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	D	−6
IV		E $\overline{U}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	D	−6
V		M Z		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	D	−6
VI		F K P R S W $\overline{E}$ $\overline{F}$ H J $\overline{K}$ $\overline{M}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t t t t t t t t	C	0
	2	f t t t t t t t t t t t t t	C	−6
	3	t f t t t t t t t t t t t t	C	−6
	4	t t f t t t t t t t t t t t	C	−6
	5	t t t f t t t t t t t t t t	C	−6
	6	t t t t f t t t t t t t t t	C	−6
	7	t t t t t f t t t t t t t t	C	−6
	8	t t t t t t f t t t t t t t	C	−6
	9	t t t t t t t f t t t t t t	C	−6
	10	t t t t t t t t f t t t t t	C	−6
	11	t t t t t t t t t f t t t t	C	−6
	12	t t t t t t t t t t f t t t	C	−6
	13	t t t t t t t t t t t f t t	C	−6
	14	t t t t t t t t t t t t f t	C	−6
	15	t t t t t t t t t t t t t f	C	−6
VII		R T $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
	3	t f t	V	−6
	4	t t f	V	−6
VIII		B		
	1	t	V	0
	2	f	V	−6
IX		Y		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6

[a] Set TRUE-FALSE switches X and *T* to TRUE for tests IV, V, and VI.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Remove the matrix assembly from the test jack.

284. Matrix Card Assembly 548532

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, J, K, P, R, T, Y, $\overline{E}$, $\overline{H}$, $\overline{L}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548532 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		P T $\overline{E}$ $\overline{H}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
II		Y J		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
III		E T $\overline{H}$ $\overline{L}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
IV		P T $\overline{E}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
V		R Y		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		E T $\overline{L}$ $\overline{T}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		P T $\overline{E}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VIII		Y $\overline{T}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IX		E T $\overline{L}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
X		K P $\overline{E}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		Y $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XII		E K $\overline{L}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Remove the matrix assembly from the test jack.

285. Matrix Card Assembly 548534

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, P, S, T, Y, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548534 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H Y		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
II		S $\overline{B}$ J $\overline{P}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
III		H $\overline{B}$ $\overline{K}$ $\overline{M}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
IV		S $\overline{B}$ $\overline{K}$ $\overline{P}$ $\overline{R}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
V		H $\overline{B}$ J $\overline{M}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VI		F P $\overline{E}$ $\overline{F}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VII		H $\overline{B}$ $\overline{P}$ $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{W}$	0
	2	f t t t t	$\overline{W}$	−6
	3	t f t t t	$\overline{W}$	−6
	4	t t f t t	$\overline{W}$	−6
	5	t t t f t	$\overline{W}$	−6
	6	t t t t f	$\overline{W}$	−6
VIII		F $\overline{E}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
IX		Y $\overline{U}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
X		J P T $\overline{E}$ $\overline{H}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XI		Y $\overline{F}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XII		E J T $\overline{H}$ $\overline{L}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Remove the matrix assembly from the test jack.

286. Matrix Card Assembly 548536

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, P, R, S, X, Y, Z, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE, and M to TRUE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548536 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		X $\overline{R}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		S Z $\overline{K}$ $\overline{P}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
III		Z $\overline{R}$ $\overline{S}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		F P S $\overline{E}$ $\overline{F}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		E R $\overline{H}$		
	1	t t t	T	0
	2	f t t	T	−6
	3	t f t	T	−6
	4	t t f	T	−6
VI		E J K $\overline{T}$		
	1	t t t t	T	0
	2	f t t t	T	−6
	3	t f t t	T	−6
	4	t t f t	T	−6
	5	t t t f	T	−6
VII		X $\overline{J}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		H Z $\overline{K}$ $\overline{R}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		H Z $\overline{J}$ $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		F H P $\overline{E}$ $\overline{F}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XI		S Y		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XII		F P $\overline{E}$ $\overline{U}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 5,100 ohms between jacks D and M.

j. Remove the matrix assembly from the test jack.

287. Matrix Card Assembly 548538

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, P, S, X, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE, and M to TRUE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548538 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		X $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
II		H Z $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches						Test point	Output voltage
III		S	Z	$\overline{K}$	$\overline{R}$				
	1	t	t	t	t			$\overline{D}$	0
	2	f	t	t	t			$\overline{D}$	−6
	3	t	f	t	t			$\overline{D}$	−6
	4	t	t	f	t			$\overline{D}$	−6
	5	t	t	t	f			$\overline{D}$	−6
IV		H	Z	$\overline{R}$	$\overline{S}$				
	1	t	t	t	t			$\overline{D}$	0
	2	f	t	t	t			$\overline{D}$	−6
	3	t	f	t	t			$\overline{D}$	−6
	4	t	t	f	t			$\overline{D}$	−6
	5	t	t	t	f			$\overline{D}$	−6
V		F	P	S	$\overline{E}$	$\overline{F}$	$\overline{R}$		
	1	t	t	t	t	t	t	$\overline{D}$	0
	2	f	t	t	t	t	t	$\overline{D}$	−6
	3	t	f	t	t	t	t	$\overline{D}$	−6
	4	t	t	f	t	t	t	$\overline{D}$	−6
	5	t	t	t	f	t	t	$\overline{D}$	−6
	6	t	t	t	t	f	t	$\overline{D}$	−6
	7	t	t	t	t	t	f	$\overline{D}$	−6
VI		X	$\overline{P}$						
	1	t	t					$\overline{W}$	0
	2	f	t					$\overline{W}$	−6
	3	t	f					$\overline{W}$	−6
VII		H	$\overline{A}$	J	$\overline{P}$	$\overline{S}$			
	1	t	t	t	t	t		$\overline{W}$	0
	2	f	t	t	t	t		$\overline{W}$	−6
	3	t	f	t	t	t		$\overline{W}$	−6
	4	t	t	f	t	t		$\overline{W}$	−6
	5	t	t	t	f	t		$\overline{W}$	−6
	6	t	t	t	t	f		$\overline{W}$	−6
VIII		S	$\overline{B}$	$\overline{M}$	$\overline{S}$				
	1	t	t	t	t			$\overline{W}$	0
	2	f	t	t	t			$\overline{W}$	−6
	3	t	f	t	t			$\overline{W}$	−6
	4	t	t	f	t			$\overline{W}$	−6
	5	t	t	t	f			$\overline{W}$	−6
IX		S	$\overline{A}$	J	$\overline{K}$	$\overline{P}$			
	1	t	t	t	t	t		$\overline{W}$	0
	2	f	t	t	t	t		$\overline{W}$	−6
	3	t	f	t	t	t		$\overline{W}$	−6
	4	t	t	f	t	t		$\overline{W}$	−6
	5	t	t	t	f	t		$\overline{W}$	−6
	6	t	t	t	t	f		$\overline{W}$	−6
X		F	P	S	$\overline{E}$	$\overline{F}$	J		
	1	t	t	t	t	t	t	$\overline{W}$	0
	2	f	t	t	t	t	t	$\overline{W}$	−6
	3	t	f	t	t	t	t	$\overline{W}$	−6
	4	t	t	f	t	t	t	$\overline{W}$	−6
	5	t	t	f	f	t	t	$\overline{W}$	−6
	6	t	t	t	f	f	t	$\overline{W}$	−6
	7	t	t	t	t	t	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 5,100 ohms between jacks M and $\overline{V}$.

j. Remove the matrix assembly from the test jack.

288. Matrix Card Assembly 548540

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, P, S, T, X, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE, and M to TRUE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548540 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches			Test point	Output voltage
I		X	$\overline{S}$			
	1	t	t		$\overline{W}$	0
	2	f	t		$\overline{W}$	−6
	3	t	f		$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
II		H $\overline{A}$ $\overline{S}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
III		S $\overline{A}$ $\overline{R}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IV		F P S $\overline{E}$ $\overline{F}$ J $\overline{M}$		
	1	t t t t t t t	$\overline{W}$	0
	2	f t t t t t t	$\overline{W}$	−6
	3	t f t t t t t	$\overline{W}$	−6
	4	t t f t t t t	$\overline{W}$	−6
	5	t t t f t t t	$\overline{W}$	−6
	6	t t t t f t t	$\overline{W}$	−6
	7	t t t t t f t	$\overline{W}$	−6
	8	t t t t t t f	$\overline{W}$	−6
V		E J T $\overline{H}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VI		E K $\overline{H}$ I		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VII		X $\overline{K}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VIII		S $\overline{A}$ J $\overline{S}$		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		F P S $\overline{E}$ $\overline{F}$ J $\overline{N}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t f t t t t t	$\overline{D}$	−6
	4	t t f t t t t	$\overline{D}$	−6
	5	t t t f t t t	$\overline{D}$	−6
	6	t t t t f t t	$\overline{D}$	−6
	7	t t t t t f t	$\overline{D}$	−6
	8	t t t t t t f	$\overline{D}$	−6
X		E J T $\overline{T}$		
	1	t t t t	$\overline{P}$	0
	2	f t t t	$\overline{P}$	−6
	3	t f t t	$\overline{P}$	−6
	4	t t f t	$\overline{P}$	−6
	5	t t t f	$\overline{P}$	−6
XI		E K $\overline{H}$ $\overline{U}$		
	1	t t t t	$\overline{P}$	0
	2	f t t t	$\overline{P}$	−6
	3	t f t t	$\overline{P}$	−6
	4	t t f t	$\overline{P}$	−6
	5	t t t f	$\overline{P}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 5,100 ohms between jacks M and $\overline{V}$.

j. Remove the matrix assembly from the test jack.

289. Matrix Card Assembly 548542

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, P, R, S, W, X, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE and M to TRUE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548542 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{A}$ $\overline{P}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
II		X $\overline{P}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
III		$\overline{A}$ $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IV		X $\overline{H}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
V		F J S $\overline{E}$ $\overline{F}$ J $\overline{K}$ $\overline{M}$		
	1	t t t t t t t t	V	0
	2	f t t t t t t t	V	−6
	3	t f t t t t t t	V	−6
	4	t t f t t t t t	V	−6
	5	t t t f t t t t	V	−6
	6	t t t t f t t t	V	−6
	7	t t t t t f t t	V	−6
	8	t t t t t t f t	V	−6
	9	t t t t t t t f	V	−6
VI		J X		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VII		F P S $\overline{E}$ $\overline{F}$ J $\overline{K}$ $\overline{M}$		
	1	t t t t t t t t	$\overline{W}$	0
	2	f t t t t t t t	$\overline{W}$	−6
	3	t f t t t t t t	$\overline{W}$	−6
	4	t t f t t t t t	$\overline{W}$	−6
	5	t t t f t t t t	$\overline{W}$	−6
	6	t t t t f t t t	$\overline{W}$	−6
	7	t t t t t f t t	$\overline{W}$	−6
	8	t t t t t t f t	$\overline{W}$	−6
	9	t t t t t t t f	$\overline{W}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		E R $\overline{T}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
IX		$\overline{A}$ $\overline{R}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
X		W X		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XI		F P $\overline{E}$ $\overline{F}$ J $\overline{M}$ $\overline{S}$		
	1	t t t t t t t	$\overline{D}$	0
	2	f t t t t t t	$\overline{D}$	−6
	3	t t t t t t t	$\overline{D}$	−6
	4	t f t t t t t	$\overline{D}$	−6
	5	t t f t t t t	$\overline{D}$	−6
	6	t t t f t t t	$\overline{D}$	−6
	7	t t t t f t t	$\overline{D}$	−6
	8	t t t t t f t	$\overline{D}$	−6
	9	t t t t t t f	$\overline{D}$	−6
XII		H $\overline{A}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 5,100 ohms between jacks M and $\overline{V}$.

j. Remove the matrix assembly from the test jack.

290. Matrix Card Assembly 548544

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, H, J, K, L, M, N, R, S, T, U, V, W, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548544 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		M R Y		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		M S $\overline{F}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
III		$\overline{H}$ $\overline{L}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IV		$\overline{J}$ $\overline{L}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		$\overline{L}$ $\overline{M}$		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
VI		$\overline{L}$ $\overline{P}$		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
VII		H Z		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		$\overline{A}$ $\overline{B}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
IX		R T Y		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		S T $\overline{F}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XI		J $\overline{A}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XII		K R $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		N $\overline{A}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIV		D L U W $\overline{C}$ $\overline{E}$ $\overline{M}$ $\overline{N}$ $\overline{V}$		
	1	t t t t t t t t t	V	0
	2	f t t t t t t t t	V	−6
	3	t f t t t t t t t	V	−6
	4	t t f t t t t t t	V	−6
	5	t t t f t t t t t	V	−6
	6	t t t t f t t t t	V	−6
	7	t t t t t f t t t	V	−6
	8	t t t t t t f t t	V	−6
	9	t t t t t t t f t	V	−6
	10	t t t t t t t t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks P and $\overline{U}$.

j. Remove the matrix assembly from the test jack.

291. Matrix Card Assembly 548546

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, E, F, H, J, P, R, S, T, X, Y, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548546 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E F Y		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
II		T X $\overline{B}$ $\overline{H}$[a]		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		D H J S Y		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IV		P R J $\overline{K}$ $\overline{P}$[a]		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		D F Y $\overline{U}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
VI		T X $\overline{B}$ $\overline{F}$[b]		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VII		S Y $\overline{M}$ $\overline{N}$ $\overline{V}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
VIII		P R J $\overline{K}$ $\overline{L}$[b]		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6

[a] Set TRUE-FALSE switches D, H, J, and Y to TRUE.

[b] Set TRUE-FALSE switches Y, $\overline{M}$, $\overline{N}$, and $\overline{V}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

292. Matrix Card Assembly 548548

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, F, J, K, L, N, P, R, S, T, Y, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{T}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548548 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		D F N Y $\overline{V}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
II		T Z $\overline{B}$ $\overline{H}$[a]		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		$\overline{S}$[a]		
	1	t	V	0
	2	f	V	−6
IV		P R J $\overline{K}$ $\overline{P}$[a]		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
V		J K L Y[b]		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VI		D F L Y $\overline{M}$ $\overline{V}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
VII		S[c]		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
VIII		T Z $\overline{B}$ F[c]		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
IX		P R J $\overline{K}$ $\overline{L}$[c]		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
X		Y $\overline{E}$ $\overline{N}$ $\overline{T}$[b]		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

[a] Set TRUE-FALSE switches J, K, L, and Y to TRUE.

[b] Set TRUE-FALSE switch S to TRUE.

[c] Set TRUE-FALSE switches Y, $\overline{E}$, $\overline{N}$, and $\overline{T}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

293. Matrix Card Assembly 548550

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches D, F, J, K, L, P, R, S, T, U, V, X, Y, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548550 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches							Test point	Output voltage
I		D	F	L	V	Y	$\overline{N}$	$\overline{V}$		
	1	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	C	−6
	6	t	t	t	t	f	t	t	C	−6
	7	t	t	t	t	t	f	t	C	−6
	8	t	t	t	t	t	t	f	C	−6
II		T	X	$\overline{B}$	$\overline{H}$[a]					
	1	t	t	t	t				W	0
	2	f	t	t	t				W	−6
	3	t	f	t	t				W	−6
	4	t	t	f	t				W	−6
	5	t	t	t	f				W	−6
III		S[a]								
	1	t							W	0
	2	f							W	−6
IV		P	R	$\overline{J}$	$\overline{K}$	$\overline{P}$[a]				
	1	t	t	t	t	t			W	0
	2	f	t	t	t	t			W	−6
	3	t	f	t	t	t			W	−6
	4	t	t	f	t	t			W	−6
	5	t	t	t	f	t			W	−6
	6	t	t	t	t	f			W	−6
V		J	K	U	Y[b]					
	1	t	t	t	t				W	0
	2	f	t	t	t				W	−6
	3	t	f	t	t				W	−6
	4	t	t	f	t				W	−6
	5	t	t	t	f				W	−6
VI		T	X	$\overline{B}$	$\overline{F}$[c]					
	1	t	t	t	t				$\overline{C}$	0
	2	f	t	t	t				$\overline{C}$	−6
	3	t	f	t	t				$\overline{C}$	−6
	4	t	t	f	t				$\overline{C}$	−6
	5	t	t	t	f				$\overline{C}$	−6
VII		P	R	$\overline{J}$	$\overline{K}$	$\overline{L}$[c]				
	1	t	t	t	t	t			$\overline{C}$	0
	2	f	t	t	t	t			$\overline{C}$	−6
	3	t	f	t	t	t			$\overline{C}$	−6
	4	t	t	f	t	t			$\overline{C}$	−6
	5	t	t	t	f	t			$\overline{C}$	−6
	6	t	t	t	t	f			$\overline{C}$	−6
VIII		S[c]								
	1	t							$\overline{C}$	0
	2	f							$\overline{C}$	−6
IX		Y	$\overline{E}$	$\overline{R}$	$\overline{U}$[b]					
	1	t	t	t	t				$\overline{C}$	0
	2	f	t	t	t				$\overline{C}$	−6
	3	t	f	t	t				$\overline{C}$	−6
	4	t	t	f	t				$\overline{C}$	−6
	5	t	t	t	f				$\overline{C}$	−6

[a] Set TRUE-FALSE switches J, K, U, and Y to TRUE.

[b] Set TRUE-FALSE switch S to TRUE.

[c] Set TRUE-FALSE switches Y, $\overline{E}$, $\overline{R}$, and $\overline{U}$ to TRUE.

Test No.	Step No.	TRUE-FALSE switches								Test point	Output voltage
X		D	F	L	U	Y	$\overline{D}$	$\overline{N}$	$\overline{V}$		
	1	t	t	t	t	t	t	t	t	$\overline{W}$	0
	2	f	t	t	t	t	t	t	t	$\overline{W}$	−6
	3	t	f	t	t	t	t	t	t	$\overline{W}$	−6
	4	t	t	f	t	t	t	t	t	$\overline{W}$	−6
	5	t	t	t	f	t	t	t	t	$\overline{W}$	−6
	6	t	t	t	t	f	t	t	t	$\overline{W}$	−6
	7	t	t	t	t	t	f	t	t	$\overline{W}$	−6
	8	t	t	t	t	t	t	f	t	$\overline{W}$	−6
	9	t	t	t	t	t	t	t	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

294. Matrix Card Assembly 548552

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches D, E, F, K, L, P, R, T, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548552 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches									Test point	Output voltage
I		D	F	L	U	X	Y	$\overline{E}$	$\overline{N}$	$\overline{V}$		
	1	t	t	t	t	t	t	t	t	t	C	0
	2	f	t	t	t	t	t	t	t	t	C	−6
	3	t	f	t	t	t	t	t	t	t	C	−6
	4	t	t	f	t	t	t	t	t	t	C	−6
	5	t	t	t	f	t	t	t	t	t	C	−6
	6	t	t	t	t	f	t	t	t	t	C	−6
	7	t	t	t	t	t	f	t	t	t	C	−6
	8	t	t	t	t	t	t	f	t	t	C	−6
	9	t	t	t	t	t	t	t	f	t	C	−6
	10	t	t	t	t	t	t	t	t	f	C	−6
II		D	F	L	U	W	Y	$\overline{A}$	$\overline{E}$	$\overline{N}$	$\overline{V}$	
	1	t	t	t	t	t	t	t	t	t	t	W	0
	2	f	t	t	t	t	t	t	t	t	t	W	−6
	3	t	f	t	t	t	t	t	t	t	t	W	−6
	4	t	t	f	t	t	t	t	t	t	t	W	−6
	5	t	t	t	f	t	t	t	t	t	t	W	−6
	6	t	t	t	t	f	t	t	t	t	t	W	−6
	7	t	t	t	t	t	f	t	t	t	t	W	−6
	8	t	t	t	t	t	t	f	t	t	t	W	−6
	9	t	t	t	t	t	t	t	f	t	t	W	−6
	10	t	t	t	t	t	t	t	t	f	t	W	−6
	11	t	t	t	t	t	t	t	t	t	f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		$\overline{S}$[a]		
	1	t	V	0
	2	f	V	−6
IV		T Z $\overline{B}$ $\overline{H}$[a]		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
V		P R J $\overline{K}$ $\overline{P}$[a]		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
VI		E K W $\overline{Y}$[b]		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		T Z $\overline{B}$ $\overline{F}$[c]		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6
VIII		P R J $\overline{K}$ $\overline{L}$[c]		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
IX		$\overline{S}$[c]		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		Y $\overline{C}$ $\overline{M}$ $\overline{R}$[b]		
	1	t t t t	$\overline{D}$	0
	2	f t t t	$\overline{D}$	−6
	3	t f t t	$\overline{D}$	−6
	4	t t f t	$\overline{D}$	−6
	5	t t t f	$\overline{D}$	−6

[a] Set TRUE-FALSE switches E, K, W, and Y to TRUE.
[b] Set TRUE-FALSE switch $\overline{S}$ to TRUE.
[c] Set TRUE-FALSE switches Y, $\overline{C}$, $\overline{M}$, and $\overline{R}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

295. Matrix Card Assembly 548554

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, P, R, S, T, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548554 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{F}$		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
II		$\overline{J}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
III		$\overline{H}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
IV		$\overline{K}$		
	1	t	$\overline{E}$	0
	2	f	$\overline{E}$	−6
V		$\overline{R}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
VI		$\overline{P}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
VII		$\overline{S}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
VIII		$\overline{T}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
IX		F		
	1	t	Z	0
	2	f	Z	−6
X		$\overline{F}$		
	1	t	Y	0
	2	f	Y	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		T		
	1	t	X	0
	2	f	X	−6
XII		R		
	1	t	W	0
	2	f	W	−6
XIII		S		
	1	t	V	0
	2	f	V	−6
XIV		P		
	1	t	U	0
	2	f	U	−6
XV		K		
	1	t	N	0
	2	f	N	−6
XVI		J		
	1	t	M	0
	2	f	M	−6
XVII		H		
	1	t	L	0
	2	f	L	−6
XVIII		E		
	1	t	D	0
	2	f	D	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{Y}$ and jacks, E, H, J, K, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

296. Matrix Card Assembly 548556

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches H, L, P, R, T, $\overline{A}$, $\overline{K}$, $\overline{L}$, $\overline{N}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548556 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H R $\overline{A}$		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
II		P R $\overline{A}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		R $\overline{A}$ $\overline{N}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
IV		R $\overline{A}$ $\overline{K}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		L R $\overline{A}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
VI		R T $\overline{A}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		R $\overline{A}$ $\overline{S}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VIII		R $\overline{A}$ $\overline{L}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

297. Matrix Card Assembly 548558

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches K, R, U, Y, $\overline{A}$, $\overline{B}$, $\overline{F}$, $\overline{H}$, J, $\overline{R}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548558 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{A}$ $\overline{F}$ $\overline{R}$		
	1	t t t	E	0
	2	f t t	E	−6
	3	t f t	E	−6
	4	t t f	E	−6
II		$\overline{A}$ $\overline{F}$ $\overline{H}$		
	1	t t t	X	0
	2	f t t	X	−6
	3	t f t	X	−6
	4	t t f	X	−6
III		K $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
IV		U $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
V		R $\overline{A}$ $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		R $\overline{A}$ J		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VII		Y		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
VIII		$\overline{B}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		Y		
	1	t	C	0
	2	f	C	−6
X		$\overline{B}$		
	1	t	V	0
	2	f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

298. Matrix Card Assembly 548560

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, N, P, R, S, T, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, J, $\overline{K}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548560 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F $\overline{N}$		
	1	t t	E	0
	2	f t	E	−6
	3	t f	E	−6
II		F $\overline{K}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6
III		F L		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
IV		F T		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		N P		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		J $\overline{L}$ $\overline{P}$ $\overline{R}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
VII		Z $\overline{R}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		J $\overline{E}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
IX		K $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{W}$	0
	2	f t t	$\overline{W}$	−6
	3	t f t	$\overline{W}$	−6
	4	t t f	$\overline{W}$	−6
X		R $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XI		$\overline{A}$ $\overline{F}$ $\overline{T}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
XII		$\overline{A}$ $\overline{F}$ J		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
XIII		H $\overline{A}$ $\overline{F}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XIV		S $\overline{A}$ F		
	1	t t t	$\overline{B}$	0
	2	f t t	$\overline{B}$	−6
	3	t f t	$\overline{B}$	−6
	4	t t f	$\overline{B}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

299. Matrix Card Assembly 548562

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, J, K, L, N, P, R, S, T, U, Y, Z, $\overline{B}$, $\overline{H}$, $\overline{L}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548562 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N P U $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
II		J N P $\overline{L}$ $\overline{R}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
III		E T Z $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
IV		L R Z $\overline{R}$		
	1	t t t t	$\overline{V}$	0
	2	f t t t	$\overline{V}$	−6
	3	t f t t	$\overline{V}$	−6
	4	t t f t	$\overline{V}$	−6
	5	t t t f	$\overline{V}$	−6
V		$\overline{B}$ $\overline{R}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
VI		N P U $\overline{L}$ $\overline{R}$ $\overline{T}$		
	1	t t t t t t	$\overline{C}$	0
	2	f t t t t t	$\overline{C}$	−6
	3	t f t t t t	$\overline{C}$	−6
	4	t t f t t t	$\overline{C}$	−6
	5	t t t f t t	$\overline{C}$	−6
	6	t t t t f t	$\overline{C}$	−6
	7	t t t t t f	$\overline{C}$	−6
VII		J N P $\overline{R}$ $\overline{S}$		
	1	t t t t t	$\overline{C}$	0
	2	f t t t t	$\overline{C}$	−6
	3	t f t t t	$\overline{C}$	−6
	4	t t f t t	$\overline{C}$	−6
	5	t t t f t	$\overline{C}$	−6
	6	t t t t f	$\overline{C}$	−6
VIII		E Z $\overline{H}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IX		K R Z $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		Y		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XI		F H		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XII		F S		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

300. Matrix Card Assembly 548564

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, J, K, P, R, S, T, U, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{H}$, J, K, P, S, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548564 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		H J Z		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
II		P S Z		
	1	t t t	$\overline{V}$	0
	2	f t t	$\overline{V}$	−6
	3	t f t	$\overline{V}$	−6
	4	t t f	$\overline{V}$	−6
III		H S Z		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		J P Z		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		T Y		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VI		Y $\overline{H}$		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6
VII		U $\overline{A}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
VIII		$\overline{A}$ $\overline{H}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
IX		T $\overline{A}$ $\overline{E}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
X		F $\overline{S}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
XI		F $\overline{K}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XII		F K		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XIII		F R		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6
XIV		F $\overline{T}$		
	1	t t	E	0
	2	f t	E	−6
	3	t f	E	−6
XV		F $\overline{J}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

301. Matrix Card Assembly 548566

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, H, K, L, N, P, R, T, U, Y, Z, $\overline{H}$, J, $\overline{K}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548566 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		N Y $\overline{S}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
II		R T $\overline{S}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
III		L R $\overline{S}$		
	1	t t t	$\overline{U}$	0
	2	f t t	$\overline{U}$	−6
	3	t f t	$\overline{U}$	−6
	4	t t f	$\overline{U}$	−6
IV		Z		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
V		N Y $\overline{K}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VI		R T $\overline{K}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6
VII		L R $\overline{K}$		
	1	t t t	C	0
	2	f t t	C	−6
	3	t f t	C	−6
	4	t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		Z		
	1	t	V	0
	2	f	V	−6
IX		F $\overline{R}$		
	1	t t	D	0
	2	f t	D	−6
	3	t f	D	−6
X		F $\overline{H}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XI		F K		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
XII		F U		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XIII		F $\overline{T}$		
	1	t t	E	0
	2	f t	E	−6
	3	t f	E	−6
XIV		F $\overline{J}$		
	1	t t	X	0
	2	f t	X	−6
	3	t f	X	−6
XV		F H		
	1	t t	$\overline{W}$	0
	2	f t	$\overline{W}$	−6
	3	t f	$\overline{W}$	−6
XVI		F P		
	1	t t	$\overline{D}$	0
	2	f t	$\overline{D}$	−6
	3	t f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

302. Special Matrix Card Assembly 548569

Note. The schematic diagram is in TM 11-5840-272-30/19.

a. Press VOLTAGES switch −50 on.

b. Press SELECT switch 1 on.

c. Insert matrix assembly 548569 into test jack J1.

d. Press the ENERGIZE switch on.

e. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{B}$		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
II		$\overline{B}$		
	1	t	$\overline{K}$	0
	2	f	$\overline{K}$	−6
III		$\overline{B}$		
	1	t	$\overline{A}$	0
	2	f	$\overline{A}$	−6
IV		$\overline{B}$		
	1	t	J	0
	2	f	J	−6
V		$\overline{B}$		
	1	t	$\overline{M}$	0
	2	f	$\overline{M}$	−6
VI		$\overline{B}$		
	1	t	$\overline{J}$	0
	2	f	$\overline{J}$	−6
VII		$\overline{B}$		
	1	t	W	0
	2	f	W	−6
VIII		$\overline{B}$		
	1	t	R	0
	2	f	R	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{B}$		
	1	t	L	0
	2	f	L	−6
X		$\overline{B}$		
	1	t	K	0
	2	f	K	−6
XI		$\overline{B}$		
	1	t	$\overline{V}$	0
	2	f	$\overline{V}$	−6
XII		$\overline{B}$		
	1	t	$\overline{R}$	0
	2	f	$\overline{R}$	−6

f. Press ENERGIZE, VOLTAGES, and SELECT switches off.

g. Remove the matrix assembly from the test jack.

h. Return all TRUE-FALSE switches to neutral positions.

303. Matrix Card Assembly 548571

Note. The schematic diagram is in TM 11–5840–272–30/19.

a. Set TRUE-FALSE switches C, D, E, F, H, J, K, L, N, P, T, U, V, W, Y, Z, $\overline{A}$, $\overline{C}$, $\overline{D}$, $\overline{F}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548571 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		C $\overline{M}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
II		D U		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
III		E K		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
IV		J $\overline{P}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
V		L V		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
VI		N W		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
VII		T Z		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
VIII		$\overline{A}$ $\overline{L}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
IX		$\overline{D}$ $\overline{F}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
X		P Y		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		$\overline{C}$ $\overline{K}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
XII		$\overline{N}$ $\overline{R}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
XIII		F $\overline{S}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
XIV		$\overline{T}$ $\overline{U}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
XV		$\overline{H}$ $\overline{V}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6
XVI		H $\overline{W}$		
	1	t t	$\overline{E}$	0
	2	f t	$\overline{E}$	−6
	3	t f	$\overline{E}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

304. Matrix Card Assembly 548573

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, M, N, P, R, S, T, Y, Z, $\overline{A}$, $\overline{H}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a LOAD between jacks U and DC VOLTAGES −50 with jumper leads, and set the LOAD selector switch to position 8.

e. Insert matrix assembly 548573 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
II		$\overline{K}$		
	1	t	W	0
	2	f	W	−6
III		N		
	1	t	V	0
	2	f	V	−6
IV		T $\overline{N}$		
	1	t t	$\overline{V}$	0
	2	f t	$\overline{V}$	−6
	3	t f	$\overline{V}$	−6
V		$\overline{H}$		
	1	t	X	0
	2	f	X	−6
VI		Y Z $\overline{A}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
VII		Y $\overline{A}$ $\overline{M}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6
VIII		Y $\overline{A}$ $\overline{L}$		
	1	t t t	U	0
	2	f t t	U	−6
	3	t f t	U	−6
	4	t t f	U	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IX		$\overline{P}$		
	1	t	E	0
	2	f	E	−6
X		R $\overline{N}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XI		$\overline{T}$		
	1	t	D	0
	2	f	D	−6
XII		F H $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		P		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
XIV		M		
	1	t	$\overline{B}$	0
	2	f	$\overline{B}$	−6
XV		K $\overline{R}$		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XVI		L S		
	1	t t	C	0
	2	f t	C	−6
	3	t f	C	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

305. Matrix Card Assembly 548575

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches H, J, K, N, P, R, S, T, U, V, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548575 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R T $\overline{E}$ $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
II		K P R $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		R T $\overline{D}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IV		K R U $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		J T $\overline{F}$ $\overline{K}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VI		J K V $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VII		J T $\overline{L}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VIII		J K N $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IX		H		
	1	t	W	0
	2	f	W	−6
X		S		
	1	t	W	0
	2	f	W	−6
XI		$\overline{H}$		
	1	t	W	0
	2	f	W	−6
XII		$\overline{J}$		
	1	t	W	0
	2	f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

306. Matrix Card Assembly 548577

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, H, J, K, N, P, R, S, T, U, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{R}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548577 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6
II		S		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6
III		$\overline{U}$		
	1	t	C	0
	2	f	C	−6
IV		$\overline{E}$		
	1	t	V	0
	2	f	V	−6
V		R T $\overline{F}$ $\overline{H}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VI		K R U $\overline{F}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VII		R T J $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VIII		K P R $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
IX		J T $\overline{F}$ $\overline{K}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
X		J K N $\overline{F}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XI		J T $\overline{L}$ $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XII		H J K $\overline{R}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

307. Matrix Card Assembly 548579

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches H, J, K, L, M, N, P, R, S, T, U, W, X, Y, Z, $\overline{A}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, and $\overline{S}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Connect a load between jack V and DC VOLTAGES −50 with jumper leads, and set LOAD switch to position 8.

e. Insert matrix assembly 548579 into test jack J1.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		R T $\overline{D}$ F		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
II		K R S $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		R T $\overline{E}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IV		K R Z $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
V		J T $\overline{F}$ $\overline{H}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VI		H J K $\overline{F}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VII		J T $\overline{P}$ $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
VIII		J K L $\overline{R}$		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
IX		M P $\overline{J}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
X		X		
	1	t	V	0
	2	f	V	−6
XI		Y $\overline{A}$ $\overline{S}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		W Y $\overline{A}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XIII		N U $\overline{M}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from the jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

308. Matrix Card Assembly 548581

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, K, L, N, P, R, S, U, W, X, Y, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548581 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E $\overline{F}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
II		U $\overline{K}$ $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
III		F W Y $\overline{H}$ $\overline{L}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
IV		Y Z $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		Y $\overline{K}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		L Y $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		Y $\overline{K}$ $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		X		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IX		P Y $\overline{K}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		E N S		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		U $\overline{A}$ $\overline{U}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XII		F L P Y $\overline{H}$ $\overline{N}$ $\overline{T}$		
	1	t t t t t t t	V	0
	2	f t t t t t t	V	−6
	3	t f t t t t t	V	−6
	4	t t f t t t t	V	−6
	5	t t t f t t t	V	−6
	6	t t t t f t t	V	−6
	7	t t t t t f t	V	−6
	8	t t t t t t f	V	−6
XIII		K U		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XIV		R $\overline{J}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XV		$\overline{E}$ $\overline{J}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

309. Matrix Card Assembly 548583

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, L, P, R, U, W, X, Z, $\overline{A}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548583 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E R		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
II		U $\overline{D}$ $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		F L P $\overline{E}$ $\overline{H}$ $\overline{S}$ $\overline{T}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
IV		H $\overline{P}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		Z $\overline{D}$ $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		$\overline{D}$ $\overline{E}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		$\overline{D}$ $\overline{E}$ $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		$\overline{D}$ $\overline{E}$ $\overline{N}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		W $\overline{D}$ $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
X		J $\overline{R}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XI		$\overline{F}$		
	1	t	V	0
	2	f	V	−6
XII		$\overline{A}$		
	1	t	V	0
	2	f	V	−6
XIII		X $\overline{J}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

310. Matrix Card Assembly 548585

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches F, J, L, R, S, U, W, X, Z, $\overline{E}$, $\overline{H}$, $\overline{L}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix card assembly 548585 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		$\overline{P}$ $\overline{R}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
II		S U $\overline{U}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		F J L W $\overline{E}$ $\overline{H}$ $\overline{T}$		
	1	t t t t t t t	$\overline{C}$	0
	2	f t t t t t t	$\overline{C}$	−6
	3	t f t t t t t	$\overline{C}$	−6
	4	t t f t t t t	$\overline{C}$	−6
	5	t t t f t t t	$\overline{C}$	−6
	6	t t t t f t t	$\overline{C}$	−6
	7	t t t t t f t	$\overline{C}$	−6
	8	t t t t t t f	$\overline{C}$	−6
IV		S Z $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		S $\overline{E}$ $\overline{M}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		S $\overline{E}$ $\overline{L}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VII		S $\overline{E}$ $\overline{S}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VIII		R S $\overline{E}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IX		$\overline{P}$ $\overline{V}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
X		X		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

311. Matrix Card Assembly 548587

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, F, U, $\overline{E}$, and $\overline{T}$ to FALSE.

b. Press VOLTAGES switch 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548587 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		E		
	1	t	D	0
	2	f	D	−6
II		F		
	1	t	W	0
	2	f	W	−6
III		$\overline{E}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IV		$\overline{T}$		
	1	t	$\overline{U}$	0
	2	f	$\overline{U}$	−6
V		U		
	1	t	$\overline{W}$	0
	2	f	$\overline{W}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks E, $\overline{E}$, and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

312. Matrix Card Assembly 548589

Note. The schematic diagram is in TM 11–5840–271–30/20.

a. Set TRUE-FALSE switches E, P, S, T, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{L}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{T}$, and $\overline{U}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548589 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		T $\overline{F}$ $\overline{U}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
II		$\overline{E}$ $\overline{L}$ $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
III		$\overline{E}$ J $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
IV		S $\overline{H}$ $\overline{U}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
V		$\overline{N}$ $\overline{R}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VI		P $\overline{N}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VII		$\overline{N}$ $\overline{P}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
VIII		E $\overline{N}$		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jacks $\overline{K}$ and $\overline{Y}$.

j. Remove the matrix assembly from the test jack.

313. Matrix Card Assembly 548591

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches F, H, J, K, L, N, P, R, S, U, Z, $\overline{A}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{X}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548591 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F $\overline{F}$ $\overline{M}$ $\overline{N}$ $\overline{R}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
II		K $\overline{L}$ $\overline{T}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
III		$\overline{U}$		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
IV		K		
	1	t	D	0
	2	f	D	−6
V		L N $\overline{K}$		
	1	t t t	D	0
	2	f t t	D	−6
	3	t f t	D	−6
	4	t t f	D	−6
VI		H P $\overline{E}$ $\overline{H}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
VII		H R $\overline{S}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6
VIII		J S U $\overline{P}$ $\overline{S}$		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6
IX		F $\overline{M}$ $\overline{R}$ $\overline{S}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
X		F L Z J $\overline{K}$ $\overline{S}$		
	1	t t t t t t	$\overline{W}$	0
	2	f t t t t t	$\overline{W}$	−6
	3	t f t t t t	$\overline{W}$	−6
	4	t t f t t t	$\overline{W}$	−6
	5	t t t f t t	$\overline{W}$	−6
	6	t t t t f t	$\overline{W}$	−6
	7	t t t t t f	$\overline{W}$	−6
XI		F $\overline{A}$ $\overline{S}$ $\overline{X}$		
	1	t t t t	$\overline{W}$	0
	2	f t t t	$\overline{W}$	−6
	3	t f t t	$\overline{W}$	−6
	4	t t f t	$\overline{W}$	−6
	5	t t t f	$\overline{W}$	−6
XII		$\overline{U}$		
	1	t	$\overline{D}$	0
	2	f	$\overline{D}$	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Return all TRUE-FALSE switches to neutral positions.

i. Measure 10,000 ohms between jack $\overline{Y}$ and jacks R, S, $\overline{E}$, $\overline{H}$, and $\overline{T}$.

j. Remove the matrix assembly from the test jack.

314. Matrix Card Assembly 548592

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, H, J, K, L, M, N, P, R, S, T, X, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, and $\overline{R}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548592 into test jack J1.

e. Connect LOAD 1 in series between jack Z and DC VOLTAGES −50 with jumper leads, and set LOAD 1 switch to position 8. Connect LOAD 2 between jack Y and DC VOLTAGES −50 with jumper leads, and set the LOAD 2 switch to position 8.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		S		
	1	t	C	0
	2	f	C	−6
II		E K T $\overline{H}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
III		H K $\overline{E}$ $\overline{F}$ $\overline{H}$		
	1	t t t t t	$\overline{V}$	0
	2	f t t t t	$\overline{V}$	−6
	3	t f t t t	$\overline{V}$	−6
	4	t t f t t	$\overline{V}$	−6
	5	t t t f t	$\overline{V}$	−6
	6	t t t t f	$\overline{V}$	−6
IV		K $\overline{H}$ $\overline{P}$		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
V		K P $\overline{H}$ $\overline{P}$		
	1	t t t t	D	0
	2	f t t t	D	−6
	3	t f t t	D	−6
	4	t t f t	D	−6
	5	t t t f	D	−6
VI		L		
	1	t	$\overline{A}$	0
	2	f	$\overline{A}$	−6
VII		E K $\overline{H}$ $\overline{P}$		
	1	t t t t	W, $\overline{W}$	0
	2	f t t t	W, $\overline{W}$	−6
	3	t f t t	W, $\overline{W}$	−6
	4	t t f t	W, $\overline{W}$	−6
	5	t t t f	W, $\overline{W}$	−6
VIII		K $\overline{H}$ $\overline{R}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		L R		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
X		J R		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XI		F L		
	1	t t	$\overline{U}$	0
	2	f t	$\overline{U}$	−6
	3	t f	$\overline{U}$	−6
XII		F J		
	1	t t	U	0
	2	f t	U	−6
	3	t f	U	−6
XIII		$\overline{K}$ $\overline{N}$ $\overline{P}$		
	1	t t t	Z	0
	2	f t t	Z	−6
	3	t f t	Z	−6
	4	t t f	Z	−6
XIV		K M P $\overline{F}$ $\overline{K}$ $\overline{N}$		
	1	t t t t t t	Z	0
	2	f t t t t t	Z	−6
	3	t f t t t t	Z	−6
	4	t t f t t t	Z	−6
	5	t t t f t t	Z	−6
	6	t t t t f t	Z	−6
	7	t t t t t f	Z	−6
XV		K P $\overline{F}$ J $\overline{M}$ $\overline{N}$		
	1	t t t t t t	Z	0
	2	f t t t t t	Z	−6
	3	t f t t t t	Z	−6
	4	t t f t t t	Z	−6
	5	t t t f t t	Z	−6
	6	t t t t f t	Z	−6
	7	t t t t t f	Z	−6
XVI		K M N X $\overline{R}$		
	1	t t t t t	Y	0
	2	f t t t t	Y	−6
	3	t f t t t	Y	−6
	4	t t f t t	Y	−6
	5	t t t f t	Y	−6
	6	t t t t f	Y	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Return all TRUE-FALSE switches to neutral positions.

k. Remove the matrix assembly from the test jack.

315. Matrix Card Assembly 548594

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches E, F, J, K, L, N, P, R, U, W, X, Z, $\overline{A}$, $\overline{B}$, $\overline{D}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{M}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, $\overline{V}$, and $\overline{W}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548594 into test jack J1.

e. Connect a load between jacks Y and ⏚ DC VOLTAGES −50 with jumper leads, and set LOAD switch to position 8.

f. Press the ENERGIZE switch on.

g. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		F J $\overline{M}$ $\overline{R}$		
	1	t t t t	C	0
	2	f t t t	C	−6
	3	t f t t	C	−6
	4	t t f t	C	−6
	5	t t t f	C	−6
II		F J P $\overline{E}$ $\overline{F}$ $\overline{U}$		
	1	t t t t t t	C	0
	2	f t t t t t	C	−6
	3	t f t t t t	C	−6
	4	t t f t t t	C	−6
	5	t t t f t t	C	−6
	6	t t t t f t	C	−6
	7	t t t t t f	C	−6
III		E F Z $\overline{A}$ $\overline{E}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
IV		E F $\overline{A}$ J $\overline{P}$		
	1	t t t t t	C	0
	2	f t t t t	C	−6
	3	t f t t t	C	−6
	4	t t f t t	C	−6
	5	t t t f t	C	−6
	6	t t t t f	C	−6
V		W $\overline{D}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VI		X $\overline{A}$		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VII		X $\overline{D}$		
	1	t t	S	0
	2	f t	S	−6
	3	t f	S	−6
VIII		W $\overline{A}$		
	1	t t	S	0
	2	f t	S	−6
	3	t f	S	−6
IX		E $\overline{B}$ $\overline{D}$ $\overline{E}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
X		E $\overline{D}$ $\overline{K}$ $\overline{P}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6
XI		L $\overline{R}$ $\overline{T}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XII		K		
	1	t	V	0
	2	f	V	−6
XIII		L P $\overline{E}$ $\overline{F}$ $\overline{V}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
XIV		R		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XV		$\overline{S}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XVI		U		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XVII		$\overline{H}$		
	1	t	$\overline{N}$	0
	2	f	$\overline{N}$	−6
XVIII		K $\overline{N}$ $\overline{M}$ $\overline{R}$ $\overline{W}$		
	1	t t t t t	Y	0
	2	f t t t t	Y	−6
	3	t f t t t	Y	−6
	4	t t f t t	Y	−6
	5	t t t f t	Y	−6
	6	t t t t f	Y	−6

h. Press ENERGIZE, VOLTAGES, and SELECT switches off.

i. Remove all jumper leads from jacks.

j. Remove the matrix assembly from the test jack.

k. Return all TRUE-FALSE switches to neutral positions.

316. Matrix Card Assembly 548596

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches B, D, E, F, H, K, L, P, R, S, U, W, X, Y, Z, $\overline{A}$, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, J, $\overline{K}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 548596 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		K P W $\overline{P}$[a]		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
II		E K X $\overline{E}$[a]		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
III		E Y $\overline{P}$[a]		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
IV		Z $\overline{R}$[a]		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
V		P $\overline{E}$ $\overline{F}$[a]		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
VI		$\overline{S}$ $\overline{T}$[a]		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VII		F $\overline{T}$[a]		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
VIII		U $\overline{H}$[a]		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
IX		B D P $\overline{P}$[a]		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
X		B E S $\overline{E}$[a]		
	1	t t t t	$\overline{C}$	0
	2	f t t t	$\overline{C}$	−6
	3	t f t t	$\overline{C}$	−6
	4	t t f t	$\overline{C}$	−6
	5	t t t f	$\overline{C}$	−6
XI		F $\overline{H}$[b]		
	1	t t	$\overline{C}$	0
	2	f t	$\overline{C}$	−6
	3	t f	$\overline{C}$	−6
XII		U $\overline{K}$ $\overline{T}$[b]		
	1	t t t	$\overline{C}$	0
	2	f t t	$\overline{C}$	−6
	3	t f t	$\overline{C}$	−6
	4	t t f	$\overline{C}$	−6
XIII		$\overline{J}$[b]		
	1	t	$\overline{C}$	0
	2	f	$\overline{C}$	−6
XIV		L P $\overline{B}$ $\overline{F}$ $\overline{N}$ $\overline{U}$		
	1	t t t t t t	V	0
	2	f t t t t t	V	−6
	3	t f t t t t	V	−6
	4	t t f t t t	V	−6
	5	t t t f t t	V	−6
	6	t t t t f t	V	−6
	7	t t t t t f	V	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
XV		E $\overline{B}$ $\overline{V}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVI		$\overline{B}$ $\overline{R}$ $\overline{V}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
XVII		H $\overline{A}$		
	1	t t	V	0
	2	f t	V	−6
	3	t f	V	−6
XVIII		L R $\overline{B}$ $\overline{V}$		
	1	t t t t	V	0
	2	f t t t	V	−6
	3	t f t t	V	−6
	4	t t f t	V	−6
	5	t t t f	V	−6

[a] Set TRUE-FALSE switch $\overline{J}$ to TRUE.
[b] Set TRUE-FALSE switches Z and $\overline{R}$ to TRUE.

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

317. Matrix Card Assembly 548598

Note. The schematic diagram is in TM 11-5840-271-30/20.

a. Set TRUE-FALSE switches B, E, H, J, K, L, M, N, P, R, S, T, Z, $\overline{B}$, $\overline{E}$, $\overline{F}$, $\overline{H}$, $\overline{J}$, $\overline{K}$, $\overline{L}$, $\overline{M}$, $\overline{N}$, $\overline{P}$, $\overline{R}$, $\overline{S}$, $\overline{T}$, $\overline{U}$, and $\overline{V}$ to FALSE.

b. Press VOLTAGES switches −50 and 50 on.

c. Press SELECT switch 1 on.

d. Insert matrix assembly 549598 into test jack J1.

e. Press the ENERGIZE switch on.

f. Make TRUE-FALSE switch settings in the sequence given in the chart below (t-true, f-false). Check the output logic voltages at the test points indicated. Return the TRUE-FALSE switches used in each test to FALSE before proceeding to the next test.

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
I		J K $\overline{L}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
II		L S $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
III		E L Z $\overline{E}$ $\overline{U}$		
	1	t t t t t	V	0
	2	f t t t t	V	−6
	3	t f t t t	V	−6
	4	t t f t t	V	−6
	5	t t t f t	V	−6
	6	t t t t f	V	−6
IV		B J $\overline{H}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
V		L $\overline{B}$ $\overline{P}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VI		L P $\overline{B}$		
	1	t t t	V	0
	2	f t t	V	−6
	3	t f t	V	−6
	4	t t f	V	−6
VII		J K $\overline{S}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6

Test No.	Step No.	TRUE-FALSE switches	Test point	Output voltage
VIII		B J $\overline{V}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
IX		L S $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
X		E L J P $\overline{U}$		
	1	t t t t t	$\overline{D}$	0
	2	f t t t t	$\overline{D}$	−6
	3	t f t t t	$\overline{D}$	−6
	4	t t f t t	$\overline{D}$	−6
	5	t t t f t	$\overline{D}$	−6
	6	t t t t f	$\overline{D}$	−6
XI		L $\overline{E}$ $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XII		L P $\overline{K}$		
	1	t t t	$\overline{D}$	0
	2	f t t	$\overline{D}$	−6
	3	t f t	$\overline{D}$	−6
	4	t t f	$\overline{D}$	−6
XIII		H N		
	1	t t	W	0
	2	f t	W	−6
	3	t f	W	−6
XIV		M R T $\overline{T}$		
	1	t t t t	W	0
	2	f t t t	W	−6
	3	t f t t	W	−6
	4	t t f t	W	−6
	5	t t t f	W	−6
XV		M T $\overline{M}$ $\overline{N}$ $\overline{R}$		
	1	t t t t t	W	0
	2	f t t t t	W	−6
	3	t f t t t	W	−6
	4	t t f t t	W	−6
	5	t t t f t	W	−6
	6	t t t t f	W	−6
XVI		T F $\overline{T}$		
	1	t t t	W	0
	2	f t t	W	−6
	3	t f t	W	−6
	4	t t f	W	−6

g. Press ENERGIZE, VOLTAGES, and SELECT switches off.

h. Remove the matrix assembly from the test jack.

i. Return all TRUE-FALSE switches to neutral positions.

By Order of the Secretary of the Army:

EARLE G. WHEELER,
General, United States Army,
Chief of Staff.

Official:
J. C. LAMBERT,
Major General, United States Army,
The Adjutant General.

Distribution:

Active Army:

DASA (6)
USASA (2)
CNGB (1)
CofEngrs (1)
TSG (1)
CSigO (5)
CofT (1)
USA CD Agcy (1)
USCONARC (5)
USAMC (5)
ARADCOM (2)
ARADCOM Rgn (2)
OS Maj Comd (3)
OS Base Comd (2)
LOGCOMD (2)
USAECOM (5)
USAMICOM (3)
USASCC (4)
MDW (1)
Armies (2)
Corps (2)
USA Corps (3)
USATC AD (2)
USATC Engr (2)
USATC Inf (2)
USATC Armor (2)
Instl (2) except Ft Monmouth (63)
Svc Colleges (2)
Br Svc Sch (2) except USADS (10)
GENDEP (OS) (2)
Sig Dep (OS) (12)
Sig Sec, GENDEP (5)
Army Dep (2) except
Ft Worth (8)
Lexington (12)
Sacramento (17)
Tobyhanna (12)
USA Elct RD Actv, White Sands (13)
USA Elct RD Actv, Ft Huachuca (2)
USA Trans Tml Comd (1)
Army Tml (1)
POE (1)
USAOSA (1)
AMS (1)
WRAMC (1)
AFIP (1)
ARMY Pic Cen (2)
USA Mbl Spt Cen (1)
USA Elct Mat Agcy (25)
Chicago Proc Dist (1)
USARCARIB Sig Agcy (1)
Sig Fld Maint Shops (3)
JBUSMC (2)
Units organized under following TOE's (2 copies each unless otherwise indicated):

9–47	11–592
9–87	11–597
9–227	44–435
9–377	44–436
9–500(Tms AA–AC)	44–437
9–510(Tms AB–CA)	44–445
11–5	44–446
11–7	44–447
11–16	44–448
11–55	44–535
11–57	44–536
11–96	44–537
11–97	44–544
11–98	44–545
11–117	44–546
11–155	44–547
11–157	44–548
11–500(Tms AA–AC & RM–RU)	
11–555	
11–557	
11–587	

NG: Units organized under following TOE: 44–545 (4)

USAR: None.

For explanation of abbreviations used, see AR 320–50.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1963—684–436